intelop

INT-1001

10/100/1000 M bit EMAC + AMBA 2.0

Product Brief, features and benefits summary

Highly customizable hardware IP block. Easily portable to Faraday-Tech's structured ASIC flow, Xilinx or Altera FPGAs

INT-1001 is highly flexible that is customizable for layer-2 through Layer-7 network security and network infrastructure applications. It is recommended for use in, among others, high performance Network security appliances and Network infrastructure appliances. It provides the key IP building block for a single high performance Giga bit Ethernet ASIC/SOC/ASSP/FPGA.

INT-1001 provides capability for enterprises to differentiate their Network security and Network infrastructure appliances from others

INT-1001 can process 1.4M packets for in-line in both directions, simultaneously, at full G-bit rate. The Direct write to Memory interface relieves the host CPU from costly DMA/buffer management execution and maintenance tasks.

- Ideal for high performance and mid performance specialized, differentiable ASICs or FPGAs for Network security or Network infrastructure applications for sustained 1G, full-duplex (2G) at 100% utilization rate processing.
- Less than 40,000 ASIC gates + on-chip memory
- Fully integrated internal RAM block, synthesizable/selectable to 16KB-256KB
- 4 intelligent DMA engines.

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G Bit High Performance MAC

- Direct Memory write and read control block, improves packet receive/transmit performance by 200-400%, by eliminating software driver to have to manage each frame and manage buffer pointers.

- Optional, On-chip DDR or SSRAM memory controller which can address 4K Bytes to 4 MB Bytes on chip or 256 MB off chip memories

- Separate User Data FIFO interface: 8/16/32/64 bit

- Host control interface: AMBA 2.0 (optional)

- Many trade-offs for some functions performed in hardware or software

- Configurable Packet Buffer size up to 256 KB for RX and TX.

- Automatic overflow into External Fast SSRAM. (optional)

- Jumbo frame support

- Same architecture scalable to 10Gbps.

  - GMII or RGMII interface

  - Sustained max packet transfer rate at 1G on Tx/Rx side;
  - 64 - 1500 Byte packets at min IFG

- Special features for Hardware TCP/IP acceleration:
  - TCP, UDP, and IP header checksum calculation for RX and TX
  - Hardware header parsing for Ethernet v2/802.3/IPv4/IPv6/PPPoE
  - TCP/IP header encapsulation and de-capsulation
  - Zero-copy delay from MAC- FIFO to application buffer

  - Host side bus can be 16 bit (100 MB) or 32/64 bit for 1Gbps
  - Programmable Rx FIFOs up to 256 K Byte
  - Programmable TX FIFOs up to 256 K bytes
  - Programmable MAC address filters
  - Statistics Counters

- 10/100 M-bit MAC with generic host side interfaces

Targeted for: ASIC, SOC, Xilinx, Altera FPGAs or ASIC design flow

  - 802.3x compliant
  - Programmable Rx FIFOs up to 64 KB
  - Programmable TX FIFOs up to 64 KB
  - Programmable MAC address filters (opt)
  - Statistics Counters (Opt)

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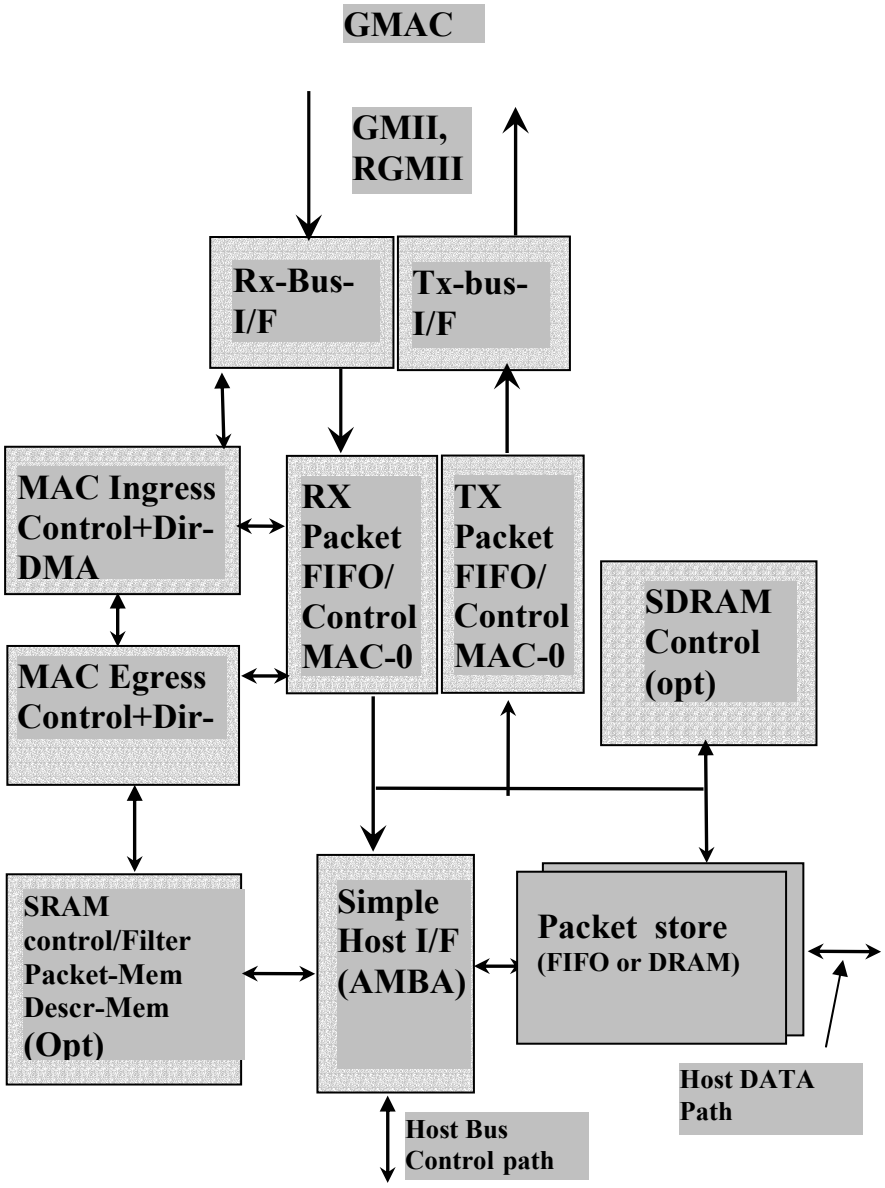
Deliverables:

- Verilog source code or Netlist.
- Verilog models for various interfaces
- Verification suite
- Test packet-traffic suite

- **Detailed specs available under NDA**



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Core Specifics				
Device Family	Virtex®-II Pro[1], Virtex-4, Virtex-5			
Speed Grades	• -5 for Virtex-II Pro • -10 for Virtex-4 • -1 for Virtex-5			
Resources Used[2]	**Slices**	**LUTs**	**FFs**	**Block RAM**
	2267	3560	3655	0
Provided with Core				
Documentation	Product Specification User Guide Getting Started Guide			
Design File Formats	EDIF and NGC netlist			
Constraints File	UCF			
Verification	VHDL test bench Verilog test fixture			
Example Design	VHDL and Verilog			
Design Tool Requirements				
Xilinx Implementation Tools	ISE® v10.1			
Simulation	Mentor ModelSim® v6.3c Cadence® IUS v6.1 Synopsys® vcs_mxY-2006.06-SP1			
Synthesis	XST 10.1			

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