
# *INT-10000*

# 10-Gbit Ethernet MAC Engine

## Product Brief, features and benefits summary

### Highly customizable hardware IP block. Easily portable to Structured ASIC flow, Custom ASICs/SoCs, Xilinx FPGAs

**INT-10000 is highly flexible that is customizable for layer-2 through Layer-7 network security and network infrastructure and other Data Networking applications. It is recommended for use in, among others, high performance Network security appliances and Network infrastructure appliances. It provides the key IP building block that is designed for easy integration with customer IPs or other standard blocks for mid performance and high performance Giga bit ASICs/SOCs/ASSPs/FPGA-SoCs.**

**INT-10000 provides capability for enterprises to differentiate their Network security and Network infrastructure appliances from others by implementing differentiated features and Performance parameters.**

**INT-10000 can process 14M packets for in-line in both directions, simultaneously, at full 10-G-bit rate. The Direct write to Memory interface relieves the host CPU from costly DMA/buffer management execution and maintenance tasks.**

- Ideal for high performance specialized, differentiable ASICs or FPGAs for Network security or Network infrastructure applications for sustained 10G, full-duplex (20G) at 100% utilization rate processing.
- Less than 40,000 ASIC gates + on-chip memory
- Designed to interface to either an off-chip PHY device or XAUI LogiCORE(Xilinx) or Altera using the XGMII Interface.
- Fully integrated internal RAM block, synthesizable/selectable to 16KB-256KB. Customizable

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- 4/8 intelligent DMA engines. Customizable.

- Direct Memory write and read control block, improves packet receive/transmit performance by 500-1000%, by eliminating software driver to have to manage each frame and manage buffer pointers.

- Optional, On-chip DDRx or SSRAM memory controller which can address 4K Bytes to 4 MB Bytes on chip or 256 MB off chip memories for packet data storage. Customizable.

- Many trade-offs for some functions performed in hardware or software

- Configurable Packet Buffer size up to 256 KB for RX and TX.
- Cut-through operation with minimum buffering for maximum flexibility in 64-bit client bus interfacing
- Configurable flow control through MAC Control pause frames that are symmetrically or asymmetrically enabled
- Programmable inter frame gap
- User side interface: AMBA, Simple, MIPs or PPC602xx
- Automatic overflow into External Fast SSRAM. (optional)

- Jumbo frame support

- Same architecture scalable to 40Gbps.

- Targeted for Xilinx, ASIC, Structured ASIC, SoC Integration
- Parameterized design for ASIC or FPGA implementation
- Complete Verification Suite
- High end Switches, Routers, security appliances
- Full 20 G bit Line rate, Packet transfer/Reception- Sustained.
- 14 M, 64 Byte Packets tested through each port
- GMII or XGMII interface
- User configurable Deep FiFOs- 16k, 32k, 64k, 256k Bytes
- Direct memory storage – interface
- Statistics counters (optional)
- Fully integrated content inspection engine (optional)
- Fully integrated CAM controller/format engine(optional)
- Configurable internal RAM block from 4KB-256KB
- Configurable Int-Host bus- 32/64/128 bits (optional)

**Deliverables:**

- Source code- Verilog
- Perl Models
- Verilog Models
- Simulation test bench
- Verification suite
- Customizable
- Netlist version

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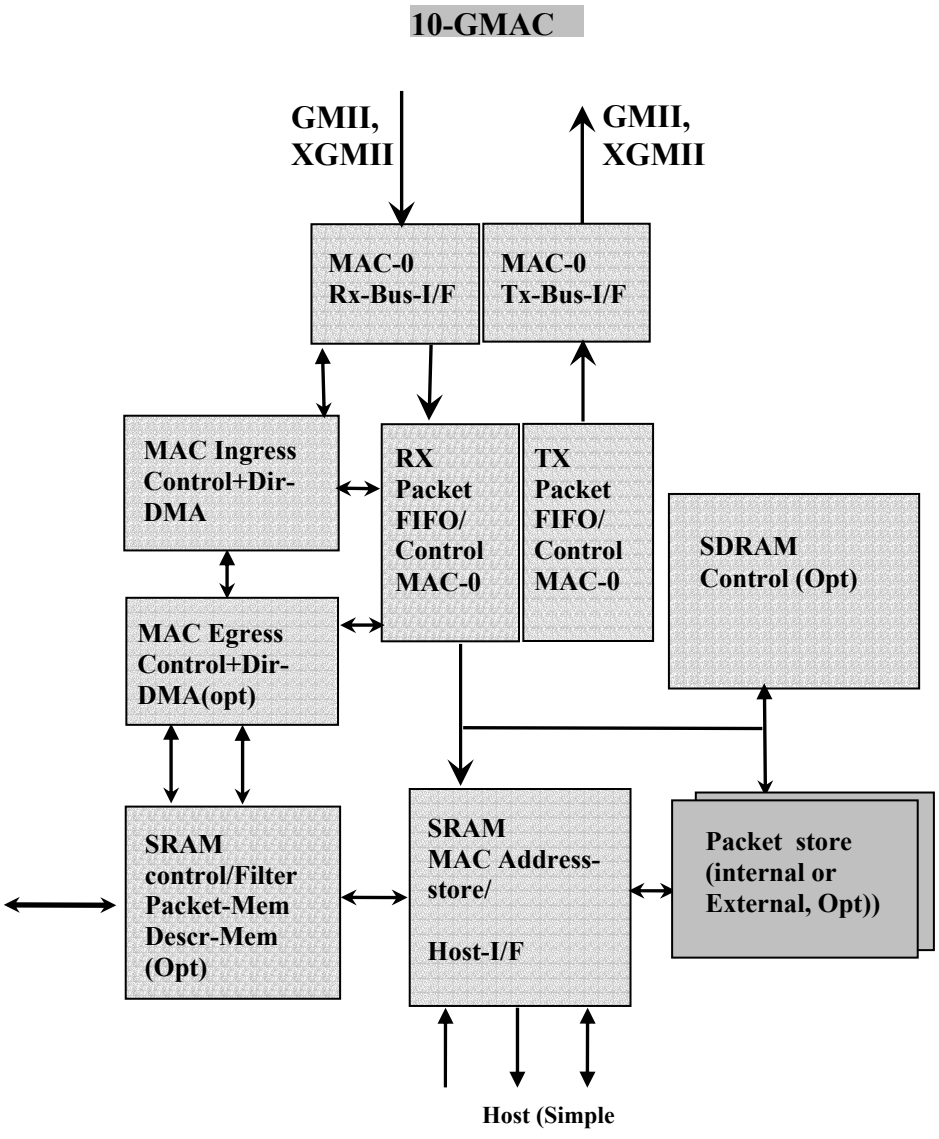


**10-G Bit MAC with Optional/customizable blocks**

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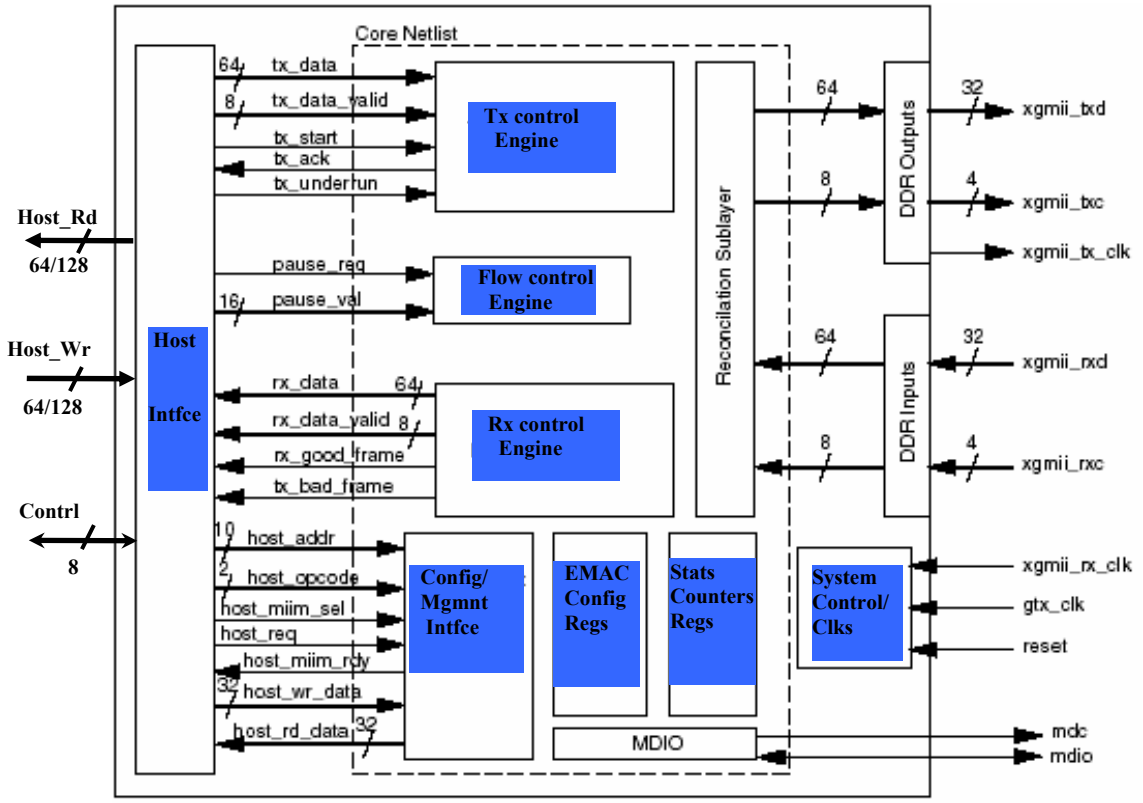


**10-G Bit MAC only, without Optional blocks**

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| Core Specifics | | | | |
|---|---|---|---|---|
| Device Family | Virtex®-II Pro[1], Virtex-4, Virtex-5 | | | |
| Speed Grades | • -5 for Virtex-II Pro<br>• -10 for Virtex-4<br>• -1 for Virtex-5 | | | |
| Resources Used[2] | **Slices** | **LUTs** | **FFs** | **Block RAM** |
| | 2267 | 3560 | 16 - 128 | 0 |
| **Provided with Core** | | | | |
| Documentation | Product Specification<br>User Guide<br>Getting Started Guide | | | |
| Design File Formats | EDIF and NGC netlist | | | |
| Constraints File | UCF | | | |
| Verification | VHDL test bench<br>Verilog test fixture | | | |
| Example Design | VHDL and Verilog | | | |
| **Design Tool Requirements** | | | | |
| Xilinx Implementation Tools | ISE® v10.1 | | | |
| Simulation | Mentor ModelSim® v6.3c<br>Cadence® IUS v6.1<br>Synopsys® vcs_mxY-2006.06-SP1 | | | |
| Synthesis | XST 10.1 | | | |

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