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# 1G bit UDP Offload Engine (UOE) MAC + Host_I/F

## *INT 1511 (Ultra-Low Latency SUOE+MAC+Host_I/F)*

## SOC IP

## Top Level Product Specifications

# Product brief, features and benefits summary:

## Highly customizable hardware IP Core. Easily portable to ASIC flow, Xilinx/Altera FPGAs or Structured/ASIC flow.

## *Provides Ultra-Low latency and highest bandwidth (NETWORK PROVEN)*

- **Latency through 1G UOE = less than 200 ns**
- **Ultra-High Throughput: Receives and Sends sustained large UDP payloads, depending upon remote server/client's capability**
- **Fully Integrated and tested on Altera/Xilinx FPGAs; UOE+MAC+Host_I/F SoC IP bundle**

**INT 1511 is the only SOC IP Core that implements a full 1G bit UDP Stack in Handcrafted, Ultra-High Performance, Innovative, Flexible and Scalable architecture which can also be easily customized for end product differentiation. It provides the lowest latency and highest performance in the industry, No exceptions…..**

**INT 1511 is also the only SOC that integrates 1G UOE + 1G EMAC + PCIe + Host_IF interfaces in the smallest logic footprint. It is highly flexible that is customizable for layer-3, layer 4-7 network infrastructure and network security systems applications. It is recommended for use in, among others, high performance Financial Servers and data center equipment design applications. It provides key IP building blocks for very high performance 1 Giga bit Ethernet ASIC/ASSP/FPGAs.**

**INT 1511 has built in advanced architectural flexibility that provides capability for enterprises to differentiate their Network infrastructure appliances from others and customize them for their specific design application.**

**INT 1511 can process UDP Session traffic for Network equipment, at 1G bit rate. This relieves the host CPU from costly UDP software related session, data copying and maintenance tasks thereby delivering 8x to 15x UDP network performance improvement when compared with UDP software.**

Intilop offers a wide range of UOE processing hardware cores for 10-GE to 1-GE applications using PCI Express or embedded system interfaces. UOE products support full UDP offload as well as conventional NIC mode operation (as an option in UDP Bypass Mode) and feature advanced PCIe/DMA software support (optional) where applications need little modification/integration to take advantage of UOE acceleration.

It provides easy-to-use frameworks for utilizing the Xilinx Virtex-5/6, Altera Stratix-IV/V and as an option, provides PCIe/DMA hardcore IPs enabling rapid and efficient system application development.

The 1G Bit UOE is based upon the proven and mature patent pending 1G bit UOE architecture from Intilop corporation.

## UOE's design version options in addition to standard UOE version:

• **Generic UOE for Network infrastructure design applications:**

a) Optional Very high performance DMA blocks also available to integrate with high performance PCIe Gen 2 interface.

b) PCIe/Driver for Linux available as option

• **UOE with enhanced features (available upon request)**

- All of the options available in Standard UOE plus;

i. IP and Port number filter block

ii. Specific IP and Port Filtered traffic routed to optional selected MAC interface/s or PCIe interface or Memory interface directly at line rate without CPU involvement.

iii. MAC Filter block, traffic routed to any of the selected interfaces

### Benefits of Intilop UOE:

Featuring APIs at different levels the General UOE allows the application developer to easily migrate from software, to UOE hardware, to custom hardware, to achieve higher performance.

Advantages and benefits of UOE

• 2 G throughput.

• Very low application to application latency

• Scalable solution; 10G, 40G

### APIs

Network applications use the Socket API. Typically OS implements the Socket API with a UDP/IP software stack. However, the Intilop UOE implements a standard Hardware API that bypasses the Kernel, places the user_payload data directly in user_space allowing next higher level applications to fully take advantage of UOEs full hardware Offload benefits.

Optionally, to achieve higher performance, Intilop has implemented an equivalent Socket API named UOE Socket API through PCIe driver which enables plug and play acceleration through a simple intercept of legacy standard calls.

• Hardware API: Enables dedicated processing in the FPGA for application specific acceleration

## 1G Bit UDP Offload Engine (UOE) – Hardware IP Core

- Ideal for Very high performance specialized, differentiable ASICs or FPGAs for Financial Applications or Network infrastructure applications

- Fully verified using comprehensive verification methodology for ASIC ports and Network system tested core.

- Smallest logic foot print; less than 30,000 Xilinx slices, Altera ALMs or 250,000 ASIC gates + on-chip memory

- Fully integrated 1 G bit high performance Ethernet MAC.

- Scalable MAC Rx FIFOs and Tx FIFOs make it ideal for optimizing system performance.

- Hardware implementation of UDP stacks' control plane and data plane.

- UDP/IP unicast or Broadcast

- Hardware implementation of ARP protocol processing.

- Hardware implementation of ICMP/Ping Replies.

- Extended ARP table creation, deletion management (optional)

- Hardware implementation of ICMP or Ping processing/Replies.

- Filters for IP addresses and UDP Port numbers

- Non-UDP Bypass mode lets all Non UDP related traffic go directly to host interface via user_fifo for UDP software to handle

- Can be deployed behind a gateway which will respond to Gateway-IP request as opposed to ARP request

- On-chip DDR or SSRAM memory controller which can address from 4K Bytes to 4 MB Bytes on chip or 256 MB off chip memories (optional)

- Simple User Side interface for easy hardware integration or a little more complicated for more power full and controlled 'Streaming' data transfers.

- Many trade-offs for some functions performed in hardware or software

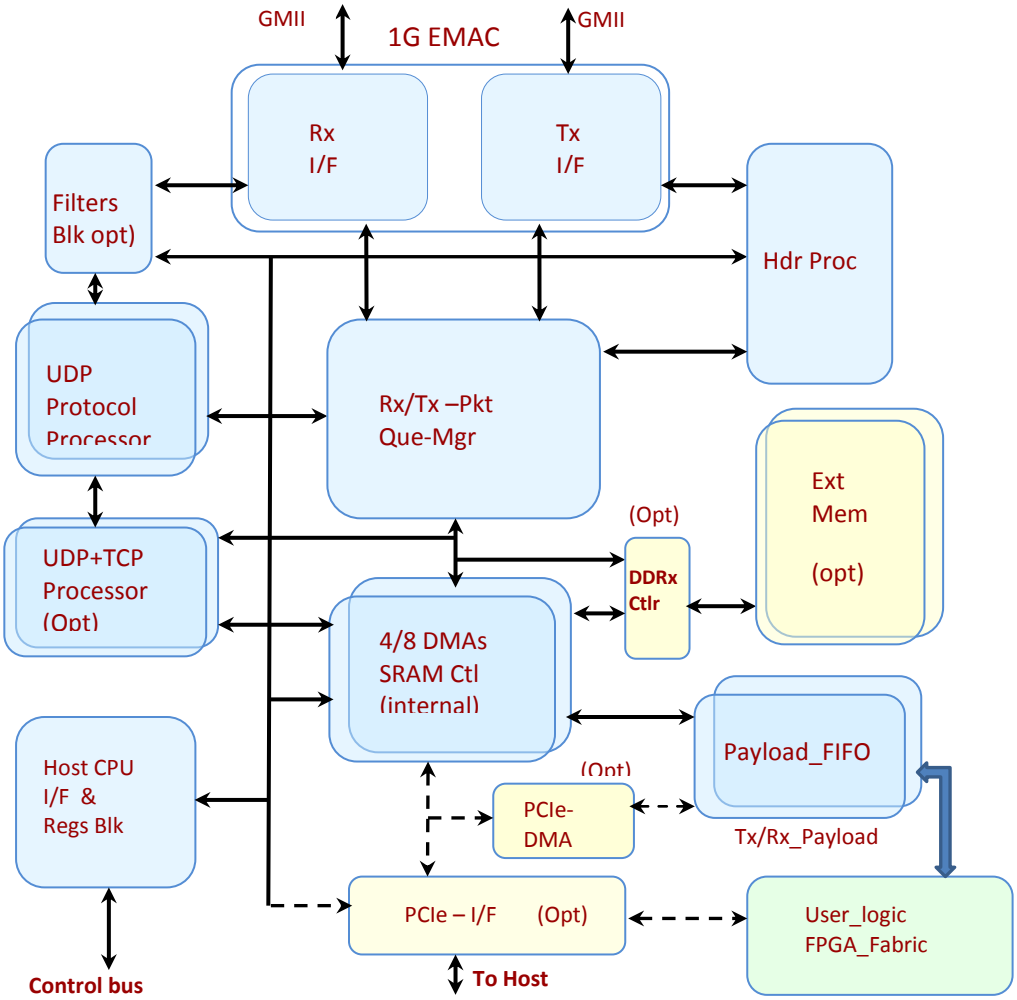
- Configurable Packet buffers, Port table buffers On-chip or Off-chip memories, attached DDRx interface. Depending on system, performance, ASIC/FPGA size requirements-> **User Customizable, (optional)**

- Interfaces directly to GMII, 1G Bit serial interfaces

- Architecture can be scaled up to 40-G bits

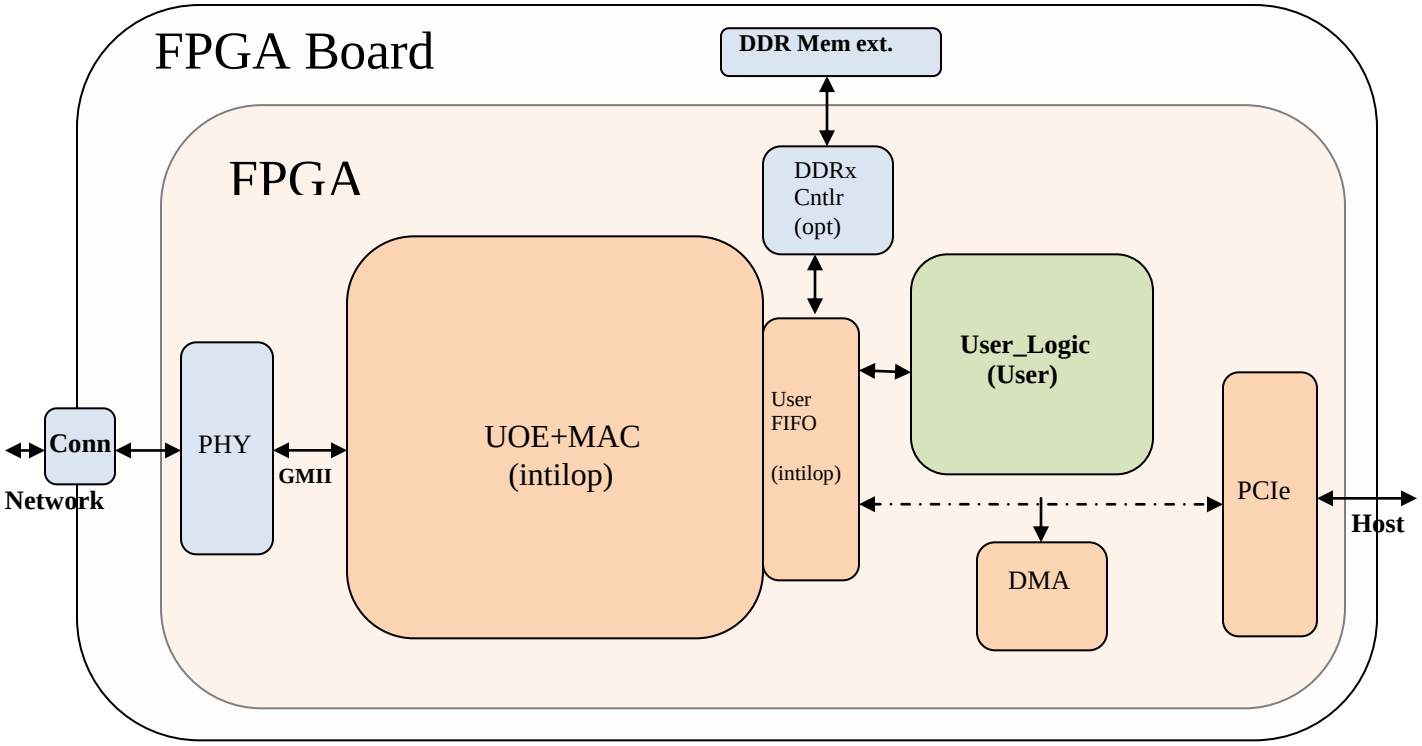
- Integrated PLB interface (Xilinx) or Altera PLB. AXI bus interface available

- Integrated AMBA 2.0 interface or MIPs CPU bus for Local Processor control. (opt)
- User programmable/prioritize-able interrupts
- Wire-speed 20-Gbps Ethernet performance in full duplex
- UDP + IP check sum generation and check performed in hardware in less than 3 clks (20 ns at 156 MHz) vs 1-2 us by typical software UDP-stack
- User programmable Session table parameters
- Dedicated set of hardware Timers for each UDP session (opt) or customizable for sharing one set of common timers for all stale sessions.
- Direct Data placement of payload data in Applications buffer at full wire speed without CPU-> reduces CPU's buffer copy time and utilization by 95%
- Support VLAN mode (optional)
- Easily customizable for filtering various IP and UDP traffic Protocols, directed towards any port or IP (Ideal for Trading Appliances)
- Implements Full UDP Offload. No CPU involvement at any stage
- Future Proof- Flexible implementation of UDP Offload
- Fully integrated and FPGA ported PHY+MAC+UOE+PCIe+Host_IF System (opt)
- Basic mini API available for easy integration with Linux/windows. Others OSs/CPUs also available
- Fully integrated SoC with PHY+MAC+UOE+PCIe/DMA and driver
- Future UDP Specs updates easily adaptable




**1G UDP Offload Engine + EMAC (Simplified Block Diagram)**

Standard UOE  UOE Options  User Design




## FPGA Development System with fully integrated and tested; PHY+MAC+UOE+PCIe+Host_IF available as an option

## *Specifications brief:*

- **Second Gen-UOE. Protocol Compliance and functionality proven in multiple networking equipment**
- **Complete header, flag processing of UDP sessions and UDP Payloads in hardware → accelerates by 8x – 15x**
- **UDP Offload Engine- 1-G b/s Wire-speed performance**
- **Scalable to 40 G b/s**
- **UDP + IP check sum- hardware**
- **UDP port address tracking/automatic DMA**
- **MAC Address search logic/filter (opt)**
- **IP address search logic/filter (opt)**
- **iRDMA implementation- Direct Data placement in Applications buffer --> reduces CPU utilization by 95+ %**
- **Future Proof- Flexible implementation of UDP Offload**
- **Accommodates future Specifications changes.**

## AMBA/PLB/AXI CPU interface features;

• Basic transfers
• Various Transfer types
• Master/slave Bus Arbitration (optional)
• Bus slave transactions
• Bus master transactions (optional)
• Address decoder
• Bus Arbiter (optional)
• System Endianness: Little-Endian

## Deliverables:

- NetList.
- Test Bench, ,vcd files, configuration code/API for easy Linux port
- Verilog models for various components e.g. UDP Client and Server models, transaction model (optional)
- External memory interface/model (optional).
- UDP Model (optional)
- Verification suite (optional)
- Test packet-traffic suite (optional)

***CONTACT INTILOP FOR LATEST SPECIFICATIONS***
***(Specifications are subject to change)***

## Technology and Solutions License Purchasing Options:

- **IP Core in Netlist form.**
- **Fully ported and Network tested FPGA development System Platform**
- **IP Customization and Customer Hardware and Application Software integration services.**

***Contact: info@ intilop.com for details***