*PCI-X Controller Model Specifications*

## Overview

Intelop PCI-X IP is set of RTL synthesizable ASIC building blocks. Designers can use these building blocks to implement PCI-X and PCI-X interface. PCI-X has been rigorously tested to ensure both PCI-X and PCI 2.3 compliance.

Intelop PCI-X IP is highly configurable and easy to integrate. The model has been proven useful in wide range of applications, like, SCSI, Fiber Channel, Gigabit Ethernet and graphics designs.

## Features

- PCI-X 1.0 and 2.0 compliant
- 32-bit or 64-bit PCI-X bus path
- 64-bit application data path
- Mutli-Master Arbiter, up to 4 masters (Optional)
- PCI 2.3 complian
- Host Bridge functionality
- Supports 0-133 MHz PCI-X bus
- Dual Address Cycles (DAC)
- Message Signaled Interrupts (MSI)
- External EEPROM support
- Easily incorporate-able as DUT with rest of the device architecture
- Synthesizable Verilog source code.

## PCI-X Application Interface

PCI-X developer controls the flow with the set of simple data and control signals. The Application interface provided by Intelop isolates the application from the complexities of PCI-X protocol and accelerates the process of integration the controller into a design.

## PCI-X Master Operations

The Master State Machine generates all master/target split transactions. It interfaces with the PCI-X Arbiter to request control of the PCI-X bus to initiate requests from the Target Sequence Controller and Message Signaled Interrupt Controller.
The Master Sequence Controller stores all defer/split transactions requested from the master, and reports any missing/error conditions received for these cycles. The Master Sequence Controller interfaces with the Master State Machine and Target State Machine, and controls the Master Defer/Split Table to support up to 32 split transactions in PCI-X mode. The Master Defer/Split Table stores all defer/split transactions requested from the master. It is controlled by the master sequence controller and interfaces with the address/data blocks. This will support 32 split transactions or 8 single address cycle deferred transactions.

## PCI-X Test Environment

Intelop provides the PCI-X Test Environment which is a set of behavioral models and test suites that simulate the performance and functionality of the PCI-X bus. The test environment allows systems designers and developers to exercise and debug the design components of the system and the system itself based upon the PCI-X standard much earlier in design cycle.
The test environment include behavioral models of PCI-X/PCI 2.3 master and target devices, a PCI-X/PCI 2.3 arbiter that controls bus access, and a protocol and timing monitor to check for and report

PCI-X/PCI 2.3 protocol and timing violations. The objective of the models is to assist in the functional verification process and reduce timing errors much before in design cycle. Additionally, Verilog source code format and examples are available on request.

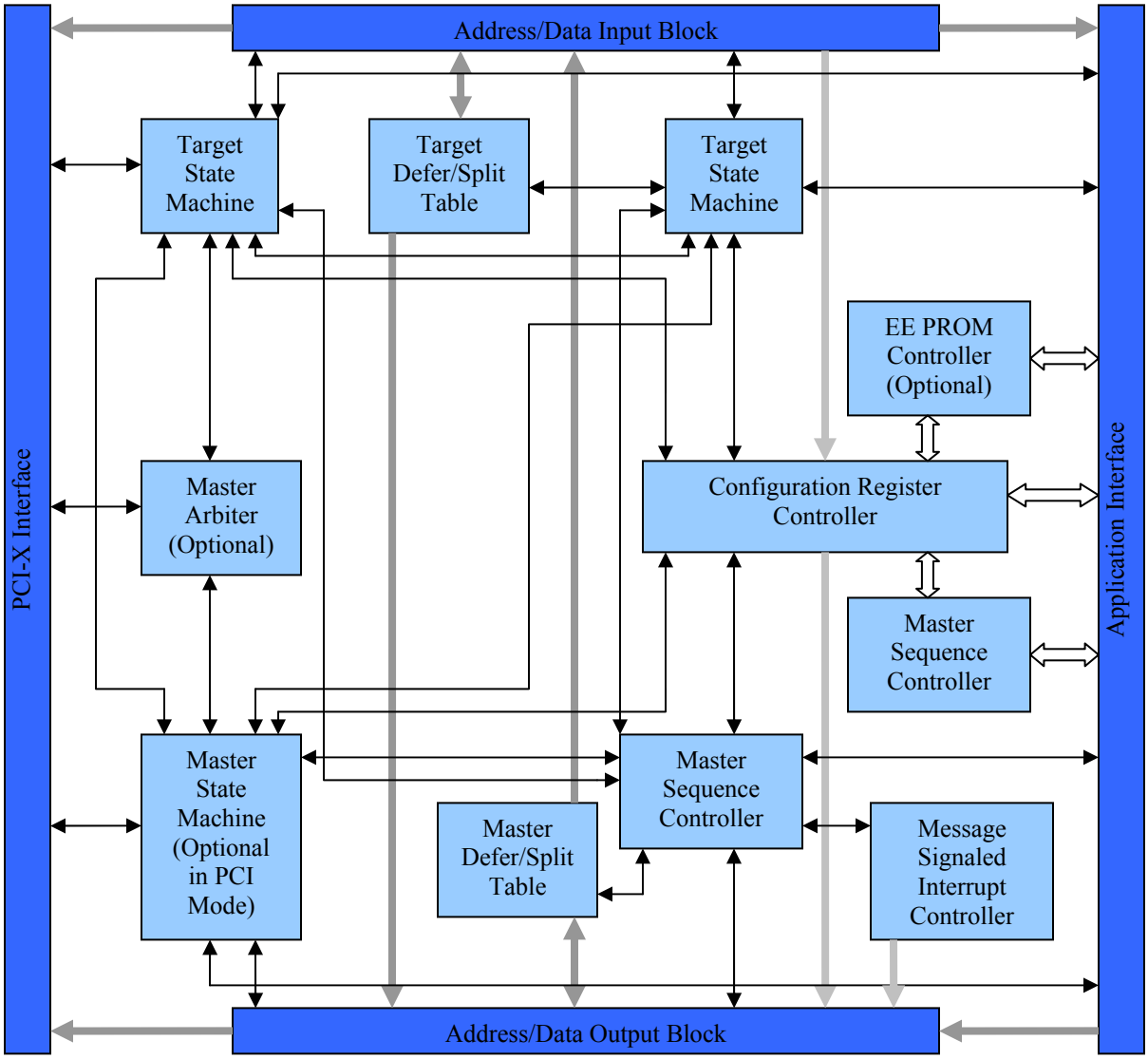


Figure: PCI Controller Block Diagram