

PCI Express Controller

Overview

Intelop PCI Express IP provides the comprehensive ASIC building blocks and builds architecture to efficiently verify PCI Express designs. IP is fully configurable to support verification of PCI Express endpoints, switches, and root complex devices. PCI Express can be configured to be verified at different levels, including 8b/10b, serial interface and PIPE interface.

Intelop PCI Express supports the System Verilog design language and the Verification Methodology Manual (VMM). The VMM defines a coverage driven methodology for SystemVerilog using a constrained random environment.

PCI Express IP can be tested as complete solution using market leading Simulation tools.

Features

- Supports x1, x2, x4, x8, x12, x16 lanes
- Verification at PIPE, 10b, and serial interface
- Automatic handling of Transaction, Data Link, and Physical layer tasks
- Full Requester and Completer functions
- Support up to eight Virtual channels
- Power management
- Automatic generation of flow control packets
- Supports and provide single word read/write transfers to memory, I/O and configuration space
- Generate block read/write transfers to memory space
- Generate message transfers
- Orders packets based on PCI Express ordering rules
- Supports transaction re-ordering and out of order completions
- Provides full access to packets at each layer
- Error injection at each layer is supported
- Provides complete functional coverage of PCI packet types
- Supports modifications and review of internal address spaces with zero cycle commands
- Supports constrained random verification with Reference Verification Methodology (RVM)
- Integrates easily into Vera, Native Testbench, Verilog and VHDL testbenches.
- Easily Synthesizable modular ASIC
- Supports most of the simulation environments.

Transceiver

It provides the automatic handling of all Transaction, Data Link and PHY layer tasks such as TLP creation and ordering, power management and link training.

As per PCI Express base specifications, Transceiver comprises a requester and completer.

Monitor (Optional)

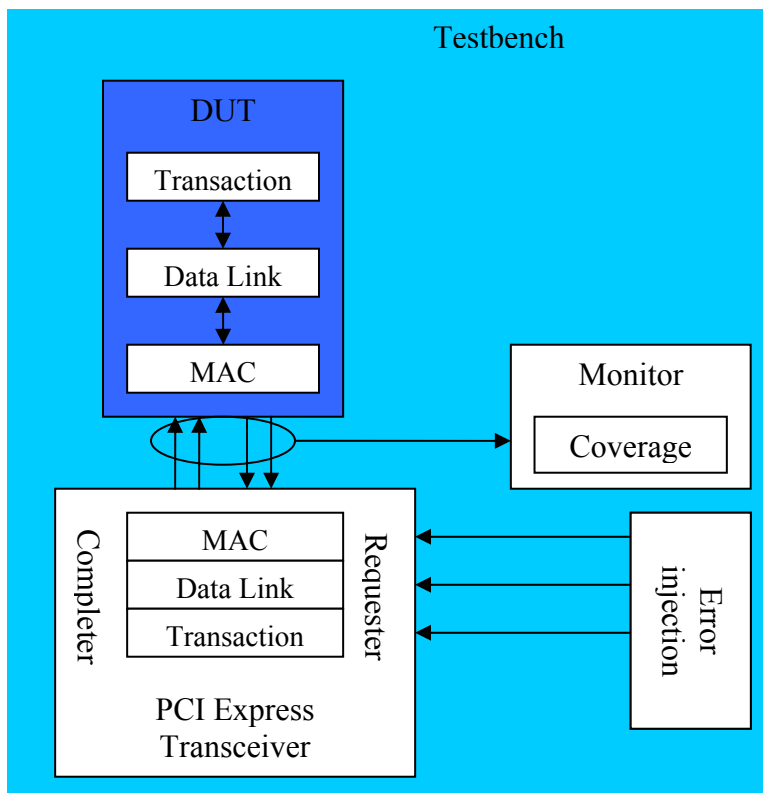
Intelop provides the optional monitor functionality that tracks verification progress including LTSSM states, PCIe transactions at the link and generation of log and coverage reports. Log files keep track of link activity and transactions at their respective occurrence. A user can also configure monitor to

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their own set of coverage groups and parameters including functional coverage and coverage verses all types of PCIe Transaction Layer Packets and Data Link Layer Packets

Benefits

- Fully Configurable IP
 - To support upstream and downstream devices including verification of endpoints, root complex and switches
 - Easy on-the-fly changes to the configuration
 - Jump to power management
 - Better link training states
- Supports Constrained Random Test
 - Simplification of test case generation by incorporating object-oriented interface.
 - Test unpredicted behavior
 - Speed up testbench development.
- Ease of use
 - Learning examples
 - Example testbenches
 - Easy to use command interface



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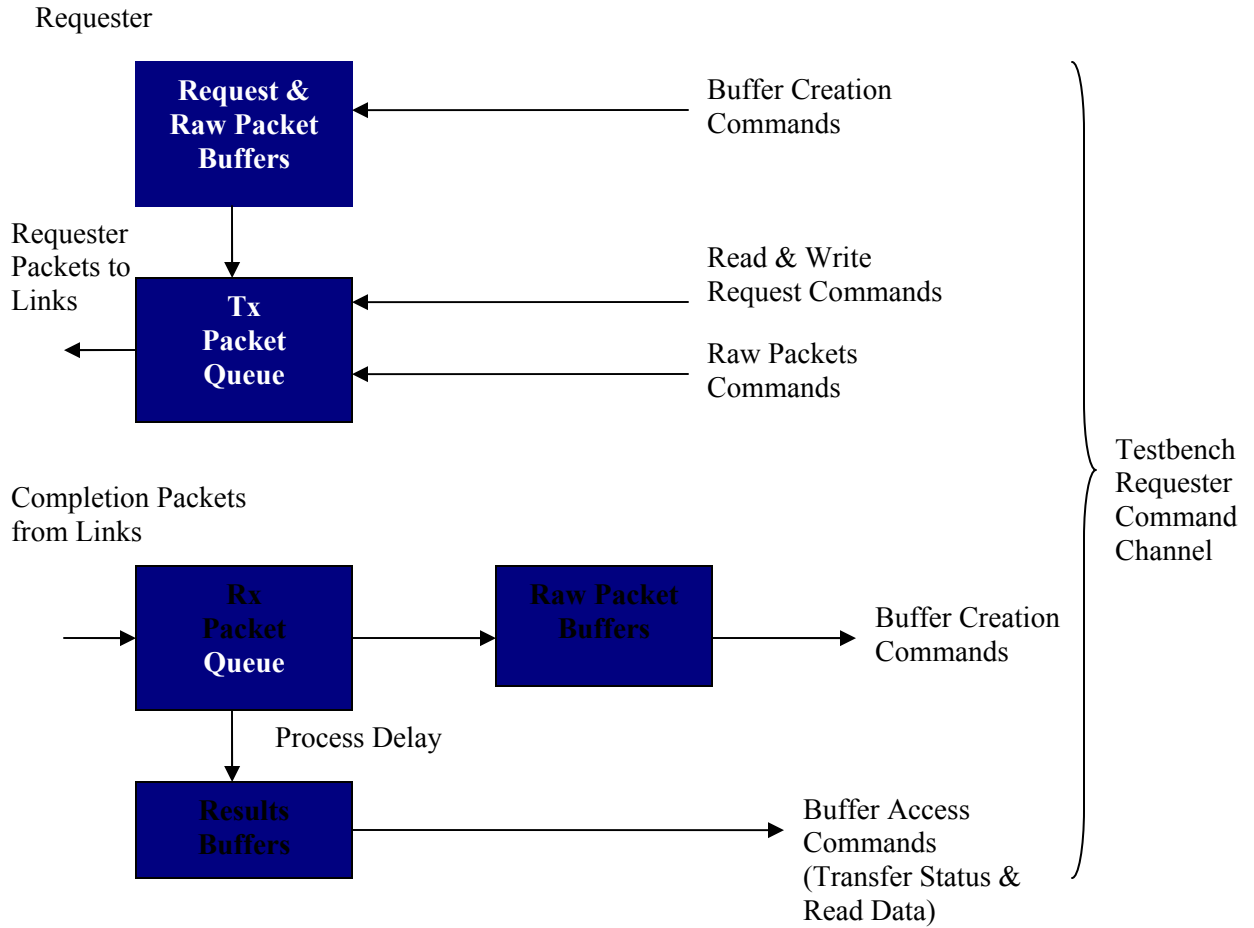


Figure: PCI Express Transceiver Verification IP Model

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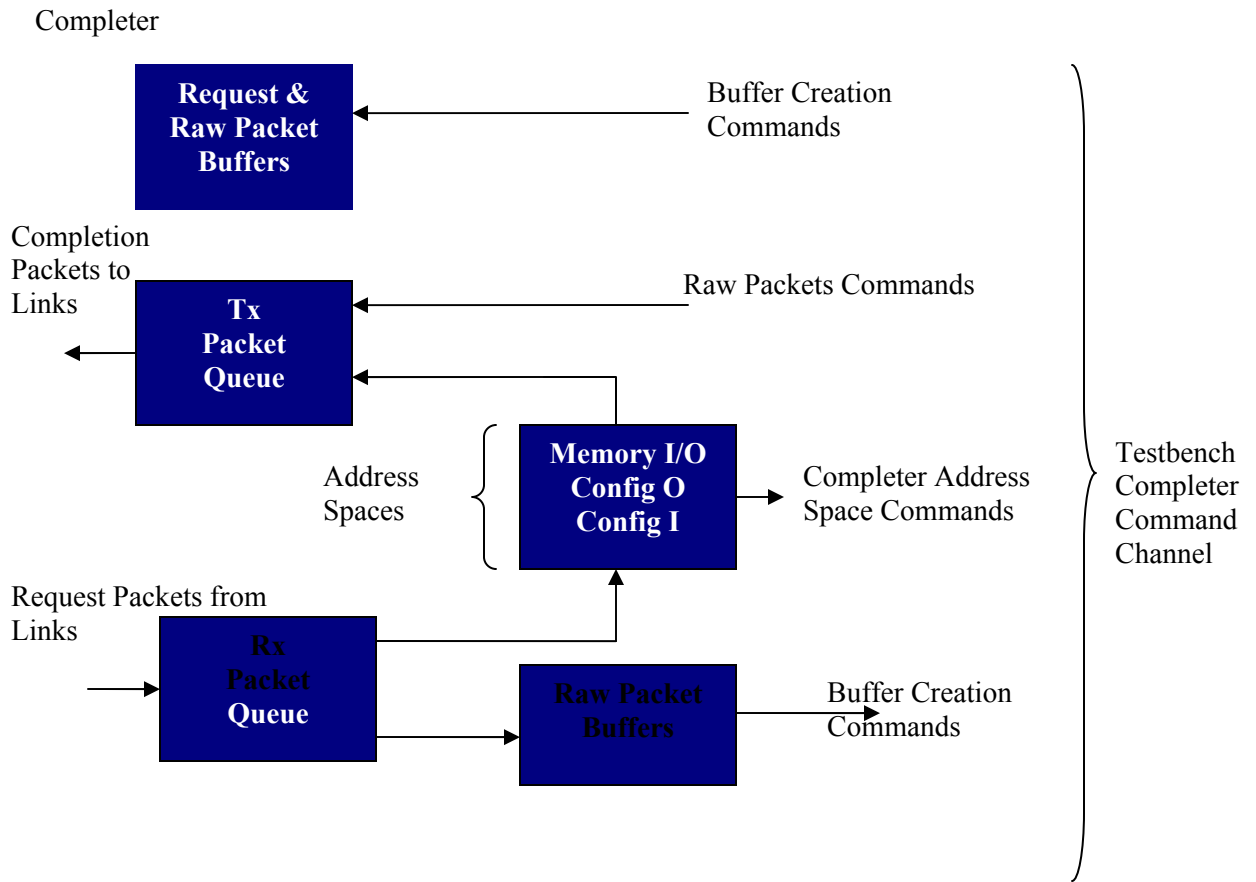


Figure: PCI Express Transceiver Verification IP Model