



A FPGA based development platform as part of an EDK is available to target intelop provided IPs or other standard IPs. The platform with Virtex-4 FX12 Evaluation Kit provides a complete hardware environment for designers to accelerate their time to market. The EDK provides a stable platform to develop and test designs targeted to Xilinx Virtex-4 FPGA family. With up to 200,000 logic cells, up to 500 MHz performance, and unrivaled system features, the EDK with a FPGA device provides a fast path to integrate and test various blocks and their functionality and performance. A ready to use platform offers clear cut advantage for validating the system concept very quickly. The current-generation FPGAs, offer a compelling cost-effective alternative to SOCs, ASICs and ASSPs. Demonstration code is included with the kit for a quick start to device familiarization.

Key Features

- Selected target-able IP code blocks that are ready for integration
- Complete FPGA product development services option
- Xilinx XC4VFX12-FF668 Virtex-4 FPGA
- Xilinx platform FLASH
- National Semiconductor DP83847 10/100 Mbps Ethernet port
- 128x64 OSRAM graphical display
- AvBus connectivity including 30 LVDS pairs
- 50-pin header for user I/O
- 8-position DIP switch
- 2 push-buttons
- 8 discrete LEDs
- 4 MB FLASH
- Micron 32 MB DDR SDRAM
- RS-232 serial port
- 100 MHz oscillator
- 8-pin DIP clock socket

Kit Includes

- Virtex-4 evaluation board
- Downloadable Documentation and Reference Design
- Wall mount power supply (5V)

VHDL source code for sample design

**As new IP blocks become available, please contact the factory for the latest updated info.*



SPECIFICATIONS:

- **Dual Processor CPU with 8KByte Cache**
 - 32 bit PPC-405, RISC ARM720T™ with 16bit instruction extensions
 - 16k/8KByte of four-way set-associative unified cache
 - MMU with 64 entry TLB
- **- DSP Co-Processor; Piccolo™**
 - 16bit multiply, accumulate instruction
 - 512Byte Instruction cache
- **Dual 10/100/1000 Mbit Ethernet MAC/PH**
- **Dual Memory Subsystem:**
 - Dynamic Memory Control
 - 16 bit multiply, accumulate instruction
 - 512Byte Instruction cache
 - 2 or 4 banks per DDR or SDRAM. Static Memory Control
 - 16/32 bit wide data path for SRAM, Flash, ROM and External I/O
 - Separate data path for LCD refresh activity
 - Five memory segments of up to 64MByte each
 - Each segment configurable as 16/32 bit
 - Programmable access time
 - 5KB on-chip dual ported SRAM for frame buffer or program/data store
 - Programmable Buzzer
 - PC Card/CompactFlash™
 - NMC1121 PC Card/CompactFlash™ controller interface
- **Dual Display Subsystem**
 - Gray Scale Controller 1
 - 640*480 pixels with 16 gray levels
 - 5Kb on-chip SRAM frame buffer
 - Single scan monochrome panel support with 1, 2, 4 bits per pixel
 - 240*160 refresh from on chip frame buffer
 - Color-Mono LCD Controller 2
 - 640*480 for color or mono STN/DSTN
 - DSTN support up to bpp (4096 colors)
 - TFT support up to bpp (4096 colors)
- **Serial Communication Subsystem**
 - 2 DMA backed UARTs



- 115Kbps
- One with modem control signals
- IrDA 115Kbps, 1.152Mbps and 4Mbps

- **Synchronous Serial Channel #1 with DMA**
 - UCB-1.1 Interface
 - Modem codec
 - Touch screen interface
 - Audio codec
 - SPI Master mode

- **Power Management Control**
 - Run mode - all functions enabled
 - Idle Mode - CPU clock shut off
 - Snooze Mode - LCD refresh from on-chip RAM
 - Standby - low power, quick transition to RUN
 - Deep Sleep - *Ultra low power*

- **System Control**
 - Two 16bit timer/counters
 - RTC interrupts at: 31.25ms, 15.62ms, 7.81ms and 3.91ms timer ticks
 - Interrupts
 - 3 external IRQ lines
 - 1 external FIQ lines
 - Programmable buzzer output
 - 32 bit real time clock (RTC)
 - 52 GPIOs including 12 column driver for keyboard
 - High speed data port, 16Mbyte/s with DMA

- **On-Chip Debug and ICE Support**
 - JTAG for Multi-ICE interface (CPU + DSP)
 - On-chip Boot ROM
 - Boot through MMC Card or Serial port

Any of the following IP blocks can be ported to run on this platform for evaluation



Usable-IP Blocks that can be integrated/customized

Hardware IP blocks; VHDL, Verilog, netlist

Network Infrastructure:

- **10/100/1000 Mbit, Tri-speed Ethernet MAC with generic host side interface**
 - Targeted for Xilinx, Altera FPGAs or ASIC design flow
 - 802.3x compliant
 - Programmable Rx FIFOs
 - Programmable TX FIFOs
 - Programmable MAC address filters
 - Statistics Counters

- **10/100 M bit MAC with generic host side interfaces**
 - Targeted for Xilinx, Altera FPGAs or ASIC design flow
 - 802.3x compliant
 - Programmable Rx FIFOs
 - Programmable TX FIFOs
 - Programmable MAC address filters
 - Statistics Counters

- **TCP/IP hardware accelerator engine for 10/100/1000 Mbit Ethernet MAC**
 - Targeted for Xilinx, Altera FPGAs or ASIC design flow
 - Decode TCP header and commands, compute TCP checksum
 - Decode I/P header and command, compute IP checksum
 - Direct interface to packet buffers
 - Direct interface to PPC-XXX processors
 - Programmable Rx FIFOs
 - Programmable TX FIFOs



Hardware IP blocks that are ported to this Platform; VHDL, Verilog, netlist

Network Security:

- **10/100/1000 Mbit, Network Search Engine Controller with generic NSE interface**

Targeted for Xilinx, Altera FPGAs or ASIC design flow

- Supports **Network Search Engines with up to 1024/512 bit wide search words**
- Support for 18 M, 9M, 4.5M NSEs
- Support for Multiple NSEs
- Support for DDR, QDR, SSRAM
- Customer user definable integrated filter block

- **10/100/1000 Mbit, Network Content Search Processor with generic interface**

Targeted for Xilinx, Altera FPGAs or ASIC design flow

- Scalable search table: 4.5 M, 9M, 18M, 36 M entries
- **Search Engines words with up to 1024/512 bit wide**
- Highly parallel, scalable architecture
- Interfaces for DDR, SSRAM
- Customer user definable integrated filter block

- **Other Network infrastructure blocks**

Targeted for Xilinx, Altera FPGAs or ASIC design flow
C-DES

- **SCALABLE C-DES core 56 bit, VHDL model of the processor, performs DES encryption and decryption.**
- **Fully compliant with FIPS46-2.**
- **Fully compliant 56-bit key DES implementation**
- **Single DES operation**
- **Encryption and decryption performed in 16/8 clock cycles**
- **Suitable for ECB, CBC, CFB and OFB implementations**
- **Suitable for Triple-DES implementation**
- **No dead clock cycles**
- **Simple interface and timing**

Bus Interface, I/O interfaces, memory Interfaces



Hardware IP blocks; VHDL, Verilog, netlist

- **64 bit/66 MHz, 32 bit/33 MHz PCI interfaces**
 - Generic host side interface
 - DDR or SDRAM interface
 - Usable in PCI to PCI bridge
 - 1 clock switch/bridge to Memory or other peripheral controllers
 - User selectable deep Rd/Wr FiFos

- **USB 2.0 interface**
 - Fully compliant to USB 2.0 specification
 - Supports full-speed 12Mbps and high-speed 480Mbps modes
 - Supports USB 2.0 Transceiver Macrocell Interface (UTMI)
 - Conformed to Virtual Component Interface Standard (VCI)
 - Programmable number of endpoints
 - Flexible endpoint configuration
 - Support for bulk, interrupt and isochronous transfers
 - Supports high-bandwidth mode
 - Optionally maximum Packet Size for bulk, interrupt and isochronous endpoints
 - Hardware enumeration manager
 - Fully-synchronous design
 - Interfaces to any application bus.

- **USB 1.1 interface**
 - Fully compliant to USB 1.1 specification
 - Conformed to Virtual Component Interface Standard (VCI)
 - Programmable number of endpoints
 - Flexible endpoint configuration
 - Support for bulk, interrupt and isochronous transfers
 - Supports high-bandwidth mode
 - Optionally maximum Packet Size for bulk, interrupt and isochronous endpoints
 - Hardware enumeration manager
 - Fully-synchronous design
 - Interfaces to any application bus.