Intelop 10Gbit Ethernet MAC Model Specifications

Introduction

Intelop provides efficient way to verify system-on-chip (SoC) designs with 10/100/1G/10G Ethernet interface. Overall Intelop Ethernet Verification IP provides following interfaces:

- Media Interface (MII)
- Serial Media Independent Interface (SMII)
- Gigabit Media Independent Interface (GMII)
- Serial Gigabit Media Independent Interface(SGMII)
- 10 Gigabit Media Independent Interface (XGMII)
- 10 Gigabit Attachment Unit Interface (XAUI)

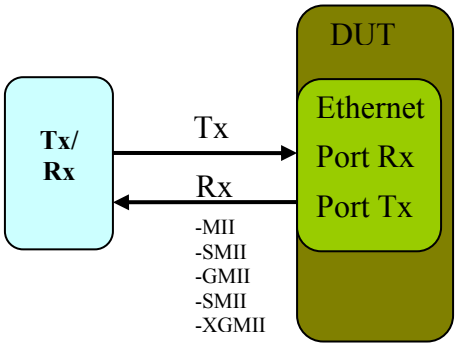
Intelop Ethernet Verification IP is compliant with IEEE 802.3 specification and verifies MAC-to-PHY layer interfaces. 10G Ethernet MAC supports 74 signal wide XGMII and 16 signal wide serial bus XAUI. The powerful bus functionality provides the capability to be interfaced with any transactor based verification environment to verify bus compliance of the DUT.

Intelop Ethernet supports the SystemVerilog design language and the Verification Methodology that defines a coverage driven methodology for SystemVerilog using a constrained random environment.

The 10G Ethernet is available in the Modelsim simulation model, synthesized EDIF and in individual suite.

Features

- Support full duplex flow control.
- Supports OC-192c PHY devices in programmable mode
- Compliant with XGMII and XAUI
- Multiple testbench and language interface
  - Verilog, VHDL and Vera
- FIFO interface on both Tx & Rx
- Supports various frame types
  - MAC, Control, Jumbo, VLAN tagging
- 64 bit internal data path
- Supports 10,000 Mb/s (10-Gbps) data transfer rates
- Most logic operates at 156.25MHz
- Protocol checking
- Programmable error injection and detection
- Reference Verification Methodology (RVM) support
- Parameterized and re-configurable MAC model



Benefits

- Enables faster and earlier testbench development and more complete verification of Ethernet designs
- Compliance for XGMII and XAUI specifications

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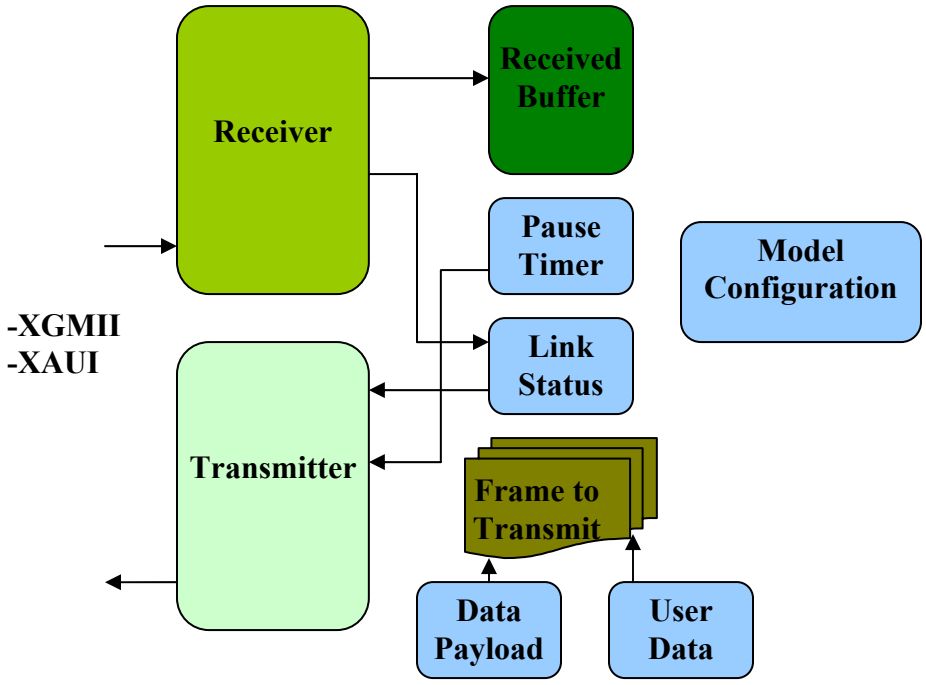
- Simplifies design cycle
- Plug-n-Play in every major simulation environment
- Design takes full advantage of the advanced verification methodology offered by major simulators



Ethernet DUT

The architecture provides the full interface capabilities to generate, receives and interprets signals on XGMII and XAUI traffic for verifying Ethernet DUT. Frame transmission is driven by user commands while reception is always active. The transmitter creates frames having different attributes with user-defined payload. The receiver remains active and watches the port to interpret all the traffic. The model configuration settings allow user to control aspects of the MAC behavior.

Compliance with Verification Methodology Manual enables reusability, consistent constrained-random environment by using coverage driven methodology to increase verification productivity and functional coverage.

Ethernet Monitor (Optional)

Intelop provides the Ethernet bus analyzer monitor. It provides the capability to check for packet size and integrity and can be interfaced with external software to receive and interpret high-level command issued by testbench. In addition it enhances the logging functionality providing full visibility for any illegal signal conditions in the transcations on the bus and logs errors appropriately. It enables sending interrupts signals to the testbench; when user-configured events occurs making it adaptive and reactive. The full visibility also provides information like source/destination addresses or payload data for testbench to handle decisions accordingly.

For more information please visit www.intelop.com

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