C68000

16-bit Microprocessor Core

The C68000 is core of a powerful 16/32-bit microprocessor and is derived from the Motorola MC68000 microprocessor. The C68000 is a fully functional 32-bit internal and 16-bit external equivalent for the MC68000. The C68000 serves interrupts and exceptions, and provides an interface for M6800 family peripherals.

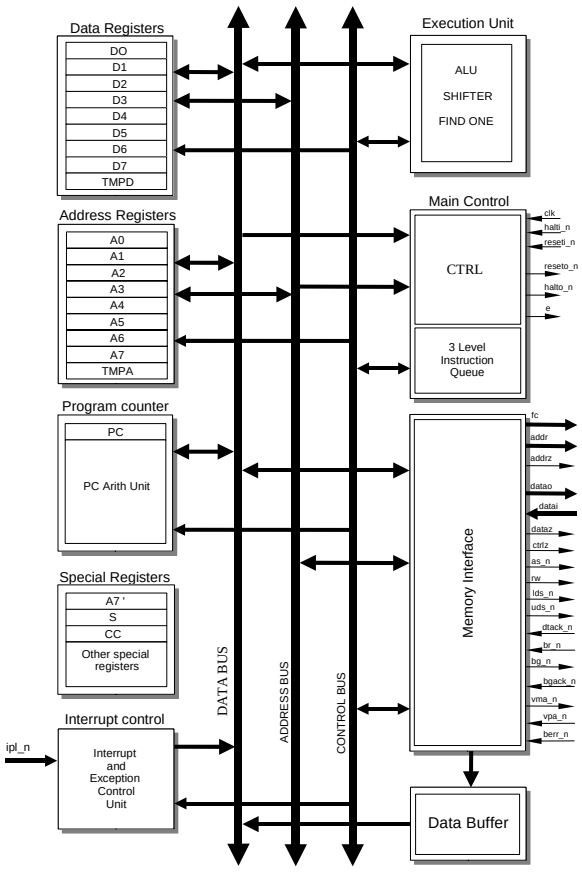
The C68000 is the microcode-free design developed for reuse in ASIC and FPGA implementations. The design is strictly synchronous without internal tri-states and with a synchronous reset. Scan insertion is straightforward.

Applications

The C68000 can be utilized for a variety of applications including:

- Microcomputer systems
- Embedded microcontroller systems
- Data computation and transfer
- Communication systems
- Professional audio and video

Block Diagram



Features

- Control Unit
  - 16-bit two levels instruction decoder
  - Three levels instruction queue
- 55 instructions and 14 address modes
- Supervisor and User mode
  - Independent stack for both modes
- Users registers
  - Eight 32-bit data & address registers
  - 16-bit status register
- Data format
  - Integer 8, 16 or 32-bit
  - BCD packet
  - Bit
- Memory interface
  - Independent data and address buses
  - Asynchronous bus control
  - 4 GB-address space
  - 31-bit address bus (optional 32-bit)
  - 8-address spaces (used 5)
  - 16-bit data bus
- Interrupt Controller
  - Seven Priority Levels
  - Unlimited interrupt sources
  - Vectored or auto-vectored interrupt modes
- Arithmetic-Logic Unit
  - 8, 16, 32-bit arithmetic and logic operations
  - Boolean manipulations
  - 16 x 16-bit multiplication (sign or unsigned)
  - 32 / 16-bit division (sign or unsigned)
- M6800 peripherals family synchronous interface
- Two or Three wire bus arbitration interface
- Operation execution is the same for data or address registers
  - No different for operation on data or address registers

March 2005

Functional Description

The C68000 core is partitioned into modules as shown above and described below.

Execution Unit

Arithmetic-Logic Unit. (ALU) performs:

- 32-bit arithmetic operations
- 32-bit logic operations
- Bit manipulations

Address/Data Shifter performs various types of shift and rotate operations by one bit position.

These two units with some additional logic, allows all basic operation on data and address registers.

Program counter

The program counter (PC) is 32 bits wide. This register can be incremented or loaded by the control unit during instruction execution.

Interrupt control

Provides seven priority levels of interrupt and calculates an internal vector during the auto-vector interrupt. It also holds the internal state of the interrupt and exception level.

Data registers

Contains eight 32-bit wide data registers (user visible). There is also a temporary data register that is invisible to the user.

Address registers

Contains eight 32-bit wide address registers (user visible). There is also a temporary data register that is invisible to the user.

Special registers

Contains the stack pointer, SR and additional special purpose registers.

Main control

Decodes and executes instructions. Contains main processor sequencer and control unit for all inner resources.

Interface

Manages all accesses to memory. Generates all control signals to memory and peripherals. This is a synchronous device working with both rising and falling edge of the *clk* (clock) signal.

Support

The core as delivered is warranted against defects for three years from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The C68000 core's functionality was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model that contained the original Motorola MC68000 chip, and the results compared with the core's simulation outputs.

Deliverables

The core includes everything required for successful implementation:

- HDL RTL source code
- Sophisticated HDL Testbench including external FIFOs, buffers, models of interfaces, and the core
- Simulation script, vectors, expected results, and comparison utility
- Constraint file
- Instantiation templates
- Synthesis script
- Comprehensive user documentation, including detailed specifications and a system integration guide

CAST
info@cast-inc.com
www.cast-inc.com

CAST, Inc. 11 Stonewall Court
Woodcliff Lake, NJ 07677 USA
tel 201-391-8300 fax 201-391-8694

evatronix
we turn engineering into art
This core developed by the processor experts at Evatronix SA.