

*intelop*



**INT-1000**

## **10/100/1Gbit Ethernet MAC Engine**

### **Product Brief, features and benefits summary**

**Highly customizable hardware IP block. Easily portable to Structured ASIC flow, Custom ASICs/SoCs, Xilinx or Altera FPGAs**

INT-1000 is highly flexible that is customizable for layer-2 through Layer-7 network security and network infrastructure applications. It is recommended for use in, among others, high performance Network security appliances and Network infrastructure appliances. It provides the key IP building block that is designed for easy integration with customer IPs or other standard blocks for mid performance and high performance Giga bit ASICs/SOCs/ASSPs/FPGA-SoCs.

INT-1000 provides capability for enterprises to differentiate their Network security and Network infrastructure appliances from others by implementing differentiated features and Performance parameters.

INT-1000 can process 1.4M packets for in-line in both directions, simultaneously, at full G-bit rate. The Direct write to Memory interface relieves the host CPU from costly DMA/buffer management execution and maintenance tasks.

- Ideal for high performance and mid performance specialized, differentiable ASICs or FPGAs for Network security or Network infrastructure applications for sustained 1G, full-duplex (2G) at 100% utilization rate processing.
- Less than 40,000 ASIC gates + on-chip memory
- Fully integrated internal RAM block, synthesizable/selectable to 16KB-256KB. Customizable
- 4/8 intelligent DMA engines. Customizable.

## G Bit High Performance MAC

- Direct Memory write and read control block, improves packet receive/transmit performance by 200-400%, by eliminating software driver to have to manage each frame and manage buffer pointers.
- Optional, On-chip DDR or SSRAM memory controller which can address 4K Bytes to 4 MB Bytes on chip or 256 MB off chip memories. Customizable.
- Many trade-offs for some functions performed in hardware or software
- Configurable Packet Buffer size up to 256 KB for RX and TX.
- Automatic overflow into External Fast SSRAM. (optional)
- Jumbo frame support
- Same architecture scalable to 10Gbps.

10/100/1000 M-bit, Tri-speed Ethernet MAC with generic host side interface  
Targeted for ASIC, SOC, Xilinx, Altera FPGAs or ASIC design flow  
o 802.3x compliant

- o GMII or RGMII interface
- o Sustained max packet transfer rate at 1G on Tx/Rx side;  
o 64 - 1500 Byte packets at min IFG
- Special features for Hardware TCP/IP acceleration:
  - o TCP, UDP, and IP header checksum calculation for RX and TX
  - o Hardware header parsing for Ethernet v2/802.3/IPv4/IPv6/PPPoE
  - o TCP/IP header encapsulation and de-capsulation
  - o Zero-copy delay from MAC- FIFO to application buffer
- o Host side bus can be 16 bit (100 MB) or 32/64 bit for 1Gbps
- o Programmable Rx FIFOs up to 256 K Byte
- o Programmable TX FIFOs up to 256 K bytes
- o Programmable MAC address filters
- o Statistics Counters
- 10/100 M-bit MAC with generic host side interfaces  
Targeted for: ASIC, SOC, Xilinx, Altera FPGAs or ASIC design flow  
o 802.3x compliant
- o Programmable Rx FIFOs up to 64 KB
- o Programmable TX FIFOs up to 64 KB
- o Programmable MAC address filters
- o Statistics Counters