



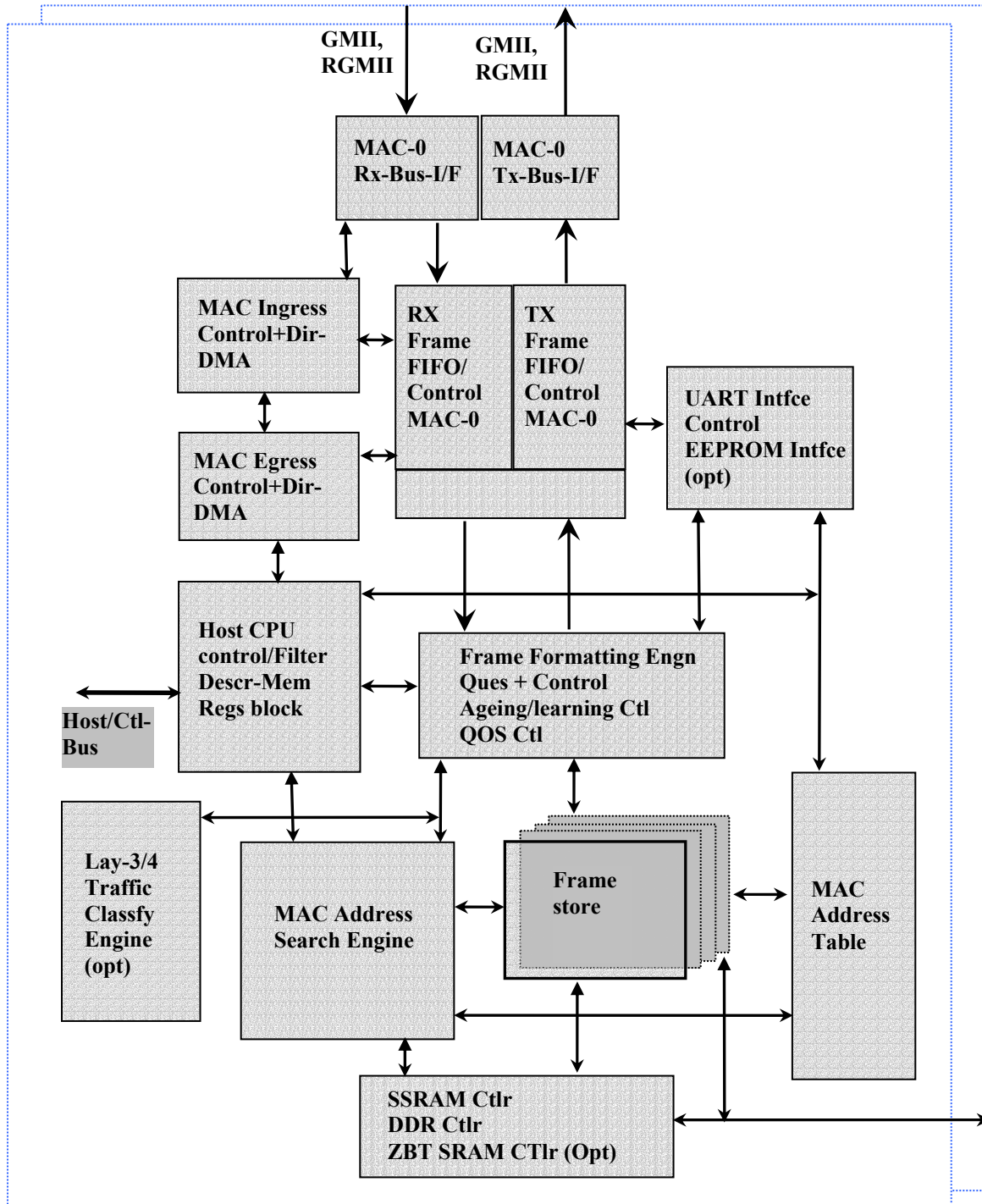
**Intelop's Switch, int-1020 is highly scalable that supports up to 16 K, 32 K or 64K MAC addresses. The internal + dedicated external memory architecture allows a very high performance packet-forwarding rate of 12 M packet per second at full wire speed. The IP core is optimized to provide a low-cost, high performance workgroup, and wiring closet layer 2 switching solution with 2/4/8 Gigabit Ethernet ports or 100 Megabit ports. Because of its flexible and scalable architecture, it can be customized to meet different features and performance requirements to meet customer's specifications e.g. support for Layer-3/4, integration with other IP cores.**

**Silicon tested in Altera and Lattice FPGAs**

## Features

- Scalable to support 2,4,8 Gigabit Ports with GMII or RGMII interface
  - Integrated 1000/100/10 Mbps MAC with its own on-chip frame buffer.
    - User selectable packet buffer size from 4 KB to 128 KB
  - Gigabit Ports can also support 100 Mbps MII interfaces
  - Host interfaces: Amba, PPC or MIPS or Generic (optional)
  - Other interfaces: PCIe: x 2, 4, 8, 16. (optional)
  - High Performance Layer 2 Packet Forwarding (12 M packets per second) and Filtering at Full-Wire Speed
    - Less than 500 ns latency for switching/learning (64 Byte packet)
    - Support for Layer-3 and Layer-4 packet classification (optional) for implementing Access control list ACLs for network security
  - Maximum throughput is 8 Gbps non-blocking
  - Customizable packet forwarding from any Port to any Port.
  - Support for jumbo packets (opt)
  - Centralized shared-memory architecture
  - Integrated packet buffers
  - Selectable Memory controllers per customer's performance/specifications e.g.
    - Internal SRAM blocks, selectable size from 4 KB to 64 KB per port, dual port or single port SRAM blocks.
    - External Fast SRAM from 256 KB to 16 M Byte - Optional
    - External DDR SDRAM or SSRAM - Optional
  - Consists of two Memory controllers at 133 MHz
  - Frame Buffer Domain: one bank of ZBT-SRAM with 1 M/2 MB total(Optional)
  - Switch Database Domain with 256 K/512 K SRAM
  - Up to 64 K MAC addresses to provide large node aggregation in wiring closet switches
  - Management interface for 'managed switching' applications
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- High end Switches, Routers, security appliances
  - Full 2 G bit Line rate, Packet transfer/Reception- Sustained.
  - Architected for 10G MAC
  - 1.6 Million, 64 Byte Packets tested through each port
  - GMII or RGMII interface
  - User configurable Deep FiFOs- 4K, 16k, 32k, 64k, 128k, 256k Bytes
  - Direct memory storage – interface

- Statistics counters
- Configurable RAM block
- Configurable Packet Bus- 32/64/128 bits
- Configurable Int-Host bus- 32/64/128 bits



### Giga-bit Multi-port Switch Architecture

**Deliverables:**

- Verilog source code or NetList.
- Verilog models for various components e.g. MAC, Memory, memory interface etc
- Verification suite
- Test packet-traffic suite

<b>Core Specifics - FPGA</b>				
Device Family	Altera Stratix III, Virtex@-II Pro <sup>1</sup> , IV, V Virtex-4, Virtex-5			
Speed Grades	<ul style="list-style-type: none"> <li>• Stratix - 2</li> <li>• -10 for Virtex-4</li> <li>• -1 for Virtex-5</li> </ul>			
Resources Used <sup>2</sup>	<b>Slices /ALMs</b>	<b>LUTs</b>	<b>FFs</b>	<b>Block RAM</b>
	~3100	~3200	~1500	16- 256
<b>Provided with Core</b>				
Documentation	Product Specification User Guide Getting Started Guide			
Design File Formats	Alter-vqm, EDIF and NGC netlist			
Constraints File	UCF			
Verification	Verilog test bench Verilog test fixture			
Example Design	Verilog			
<b>Design Tool Requirements</b>				
Xilinx/Altera Implementation Tools	Quartus 8.1 ISE@ v10.1			
Simulation	Mentor ModelSim@ v6.3c Cadence@ IUS v6.1 Synopsys@ vcs_mxY-2006.06-SP1			
Synthesis	Quartus 8.1 XST 10.1			