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1G bit TCP Offload Engine + PCIe/DMA SOC IP

INT 2012 (Ultra-Low Latency STOE+PCIe/DMA)

Top Level Product Specifications

Product brief, features and benefits summary:

Highly customizable hardware IP block. Easily portable to ASIC flow, Xilinx/Altera FPGAs or Structured/ASIC flow.

Second Generation TOE and System Solutions provide 'Ultra-Low Latency' and Ultra-High Performance with highest TCP bandwidth in Full Duplex. Network Tested and TCP protocol proven.

- **Latency through 1 G TOE = less than 100 ns**
- **Ultra-High Throughput, Full Duplex: Receives and Sends sustained large TCP payloads, depending upon remote server/client's capability**
- **Fully Integrated and tested on Altera/Xilinx FPGAs; TOE+MAC+PCIe/DMA SoC IP bundle.**

INT 2012 is the only SOC IP Core that implements a full 1G bit TCP Stack in Handcrafted, Ultra-Low Latency and Very High Performance, Innovative, Flexible and Scalable architecture which can also be easily customized for end product differentiation.

INT 2012 is the only SOC that integrates 1G TOE + MAC + PCIe/DMA + Host interfaces in the smallest logic footprint. It is highly flexible that is customizable for layer-3, layer 4-7 network infrastructure and network security systems applications. It is recommended for use in, among others, high performance Servers, NICs, SAN/NAS and data center equipment design applications. It provides key IP building blocks for very high performance 1-Giga bit Ethernet ASIC/ASSP/FPGAs.

INT 2012 has built in advanced architectural flexibility that provides capability for enterprises to differentiate their Network security and Network infrastructure appliances from others and customize them for their specific design application.

INT 2012 can process TCP/IP sessions as client/server in mixed session mode for Network equipment and in-line network security appliances, simultaneously, at 1-G-bit rate. This relieves the host CPU from costly TCP/IP software related session setup/tear down, data copying and maintenance tasks thereby delivering 8x to 15x TCP/IP network performance improvement when compared with TCP/IP software.

Intilop offers a wide range of TOE processing hardware cores for 1GE to 10GE applications using PCI Express or embedded system interfaces. TOE products support full TCP offload as well as conventional NIC mode operation (as an option in TCP Bypass Mode) and feature advanced PCIe/DMA software support (optional) where applications need little modification/integration to take advantage of TOE acceleration.

It provides easy-to-use frameworks for utilizing the Xilinx Virtex-5/6, Altera Stratix-IV/V and as an option, PCIe/DMA hardcore IPs enabling rapid and efficient system application development.

The 1 G Bit TOE is based upon the proven and mature patent pending 1 G bit TOE architecture from Intilop corporation.

The same architecture is scalable to 10G and 40G bit.

TOE's design versions-

• **Generic TOE for Network infrastructure design applications:**

a) 16 Session with Payload FIFO of 8/16/32 K bytes

b) 32 Session with Payload FIFO of 8/16/32 K bytes

c) 64 Session with scalable Payload FIFO of 8/16/32 K bytes.

d) 128 Session with scalable Payload FIFO of 8/16/32 K bytes

e) 128+ Sessions depend upon on-chip memory

f) Optional Very high performance DMA blocks also available to integrate with high performance PCIe Gen 2 interface.

g) PCIe/Driver for Linux available as option

• **TOE with enhanced Security features (available upon request)**

- All of the options available in Generic TOE plus;

i. Protocol filter block can selectively direct traffic for any known application level protocol to any selected MAC port; e.g. all IM/chat traffic, SMTP (email), Web(http) traffic, VoIP etc. can be filtered and directed to selected ports.

ii. IP and Port number filter block

iii. Specific IP and Port Filtered traffic routed to optional selected MAC interface/s or PCIe interface or Memory interface directly at line rate without CPU involvement.

iv. MAC Filter block, traffic routed to any of the selected interfaces

Benefits of Intilop TOE:

Full TCP Offload with API which allows the application developer to easily migrate from TCP/IP Software to TOE hardware, achieving Ultra-high performance.

• 1G throughput.

• Very low application to application latency

• Scalable solution; 10G, 40G

APIs

Network applications use the Socket API. Typically OS implements the Socket API with a TCP/IP software stack. However, the Intilop TOE implements a standard Hardware API that bypasses the Kernel, places the user_payload data directly in user_space allowing next higher level applications to fully take advantage of TOEs full hardware Offload benefits.

Optionally, to achieve higher performance, Intilop has implemented an equivalent Socket API named TOE Socket API through PCIe driver which enables plug and play acceleration through a simple intercept of legacy standard calls.

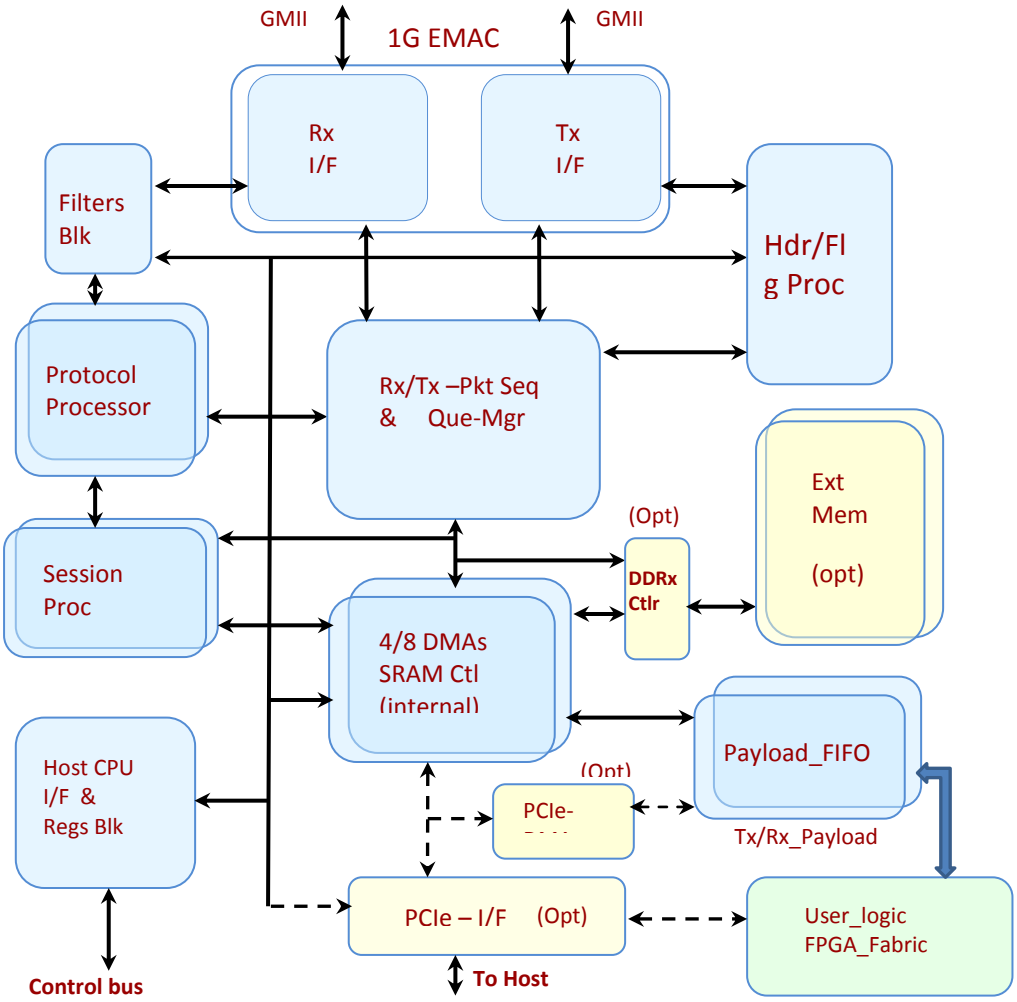
• Hardware API: Enables dedicated processing in the FPGA for application specific acceleration

- Ideal for Very high performance specialized, differentiable ASICs or FPGAs for Network security or Network infrastructure applications
- Fully verified using comprehensive verification methodology for ASIC ports and Network system tested core.
- Smallest logic foot print; less than 30,000 Xilinx slices, Altera ALMs or 250,000 ASIC gates + on-chip memory
- Fully integrated 10 G bit high performance Ethernet MAC.
- Scalable MAC Rx FIFOs and Tx FIFOs make it ideal for optimizing system performance.
- Hardware implementation of TCP/IP stacks' control plane and data plane.
- Hardware implementation of ARP protocol processing.
- Extended ARP table creation, deletion management (optional)
- Adheres to RFCs; 793, 1500, 1700, 813, 791, 2001
- Hardware implementation of ICMP or Ping processing.
- 'Sliding Window'. Similar mechanism implemented in hardware allowing Flow Control
- 'Slow start' transfer control in hardware (opt)
- Customizable for IP-protocol only.
- Non-TCP Bypass mode lets all Non TCP/IP related traffic go directly to host interface via user_fifo for TCP/IP software to handle
- Can be deployed behind a gateway which will respond to Gateway-IP request as opposed to ARP request
- On-chip DDR or SSRAM memory controller which can address from 4K Bytes

to 4 MB Bytes on chip or 256 MB off chip memories (optional)

- Simple User Side interface for easy hardware integration or a little more complicated for more power full and controlled 'Streaming' data transfers.
- Many trade-offs for some functions performed in hardware or software
- Configurable Packet buffers, session table buffers On-chip or Off-chip memories, attached DDR I/II interface. Depending on system, performance, ASIC/FPGA size requirements-> **User Customizable, (optional)**
- Interfaces directly to XGMII, 10 G Bit serial interfaces
- Architecture can be scaled up to 40-G bits
- Customizable to handle jumbo frames
- Integrated PLB interface (Xilinx) or Altera PLB. AXI bus interface available
- Integrated AMBA 2.0 interface or MIPs CPU bus for Local Processor control. (opt)
- User programmable/prioritize-able interrupts
- Performs connection/session management
- Monitors, Stores, Maintains and processes up to 1024 live TCP sessions. Customizable to implement more, depending upon on-chip memory availability and other FPGA limitations.
- Extendable to 4K TCP sessions. Internal Memory dependent.
- Wire-speed 2-Gbps Ethernet performance in full duplex
- Multiple TOEs can process up to 4K connections per second
- TCP + IP check sum generation and check performed in hardware in less than 4 clks (32 ns at 125 MHz) vs 1-2 us by typical software TCP-stack
- Connection Set up, tear down/termination and TCP data transfer without CPU involvement.
- User programmable Session table parameters
- Dedicated set of hardware Timers for each TCP/IP session (opt) or customizable for sharing one set of common timers for all stale sessions.
- Multiple 'slot storage' for fragmented packets. More slots allocated when more On-chip Memory available. Self-checking available memory logic. (optional)
- Out of sequence packet detection/storage and Reassembly/Segmentation (optional)
- Direct Data placement in Applications buffer at full wire speed without CPU-> reduces CPU's buffer copy time and utilization by 95%

- Support VLAN mode (optional)
- Easily customizable for filtering various IP and TCP traffic Protocols, directed towards any port or IP (Ideal for security appliances)
- Implements Full TCP/IP Offload. No CPU involvement at any TCP stage
- Future Proof- Flexible implementation of TCP Offload
- Fully integrated and FPGA ported PHY+MAC+TOE+PCIe/DMA System (opt)
- Basic mini API available for easy integration with Linux/windows. Others OSs/CPUs also available
- Fully integrate System with MAC+TOE+PCIe/DMA and driver
- Future TCP Specs updates easily adaptable



1G TCP Offload Engine + EMAC (Simplified Block Diagram)

Standard TOE TOE Options User Design

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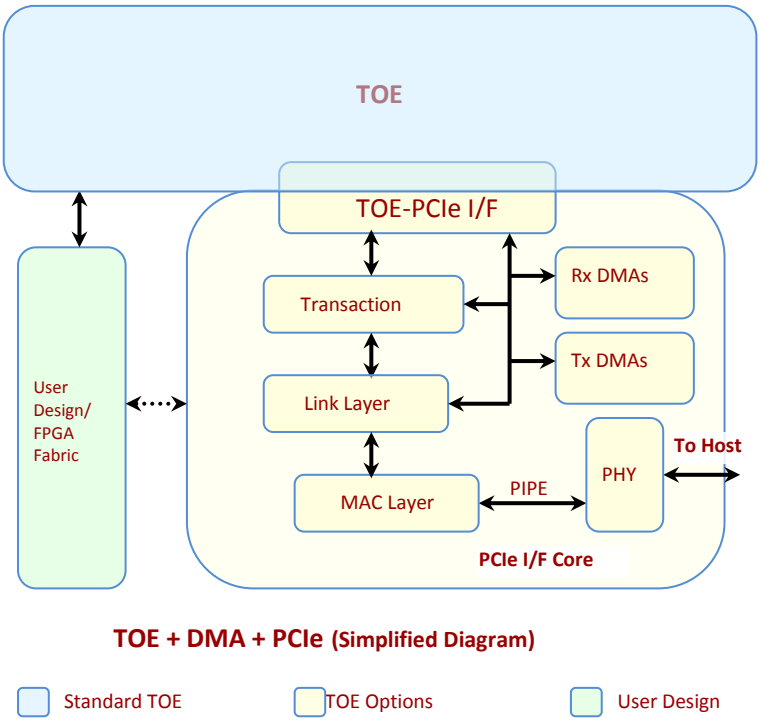
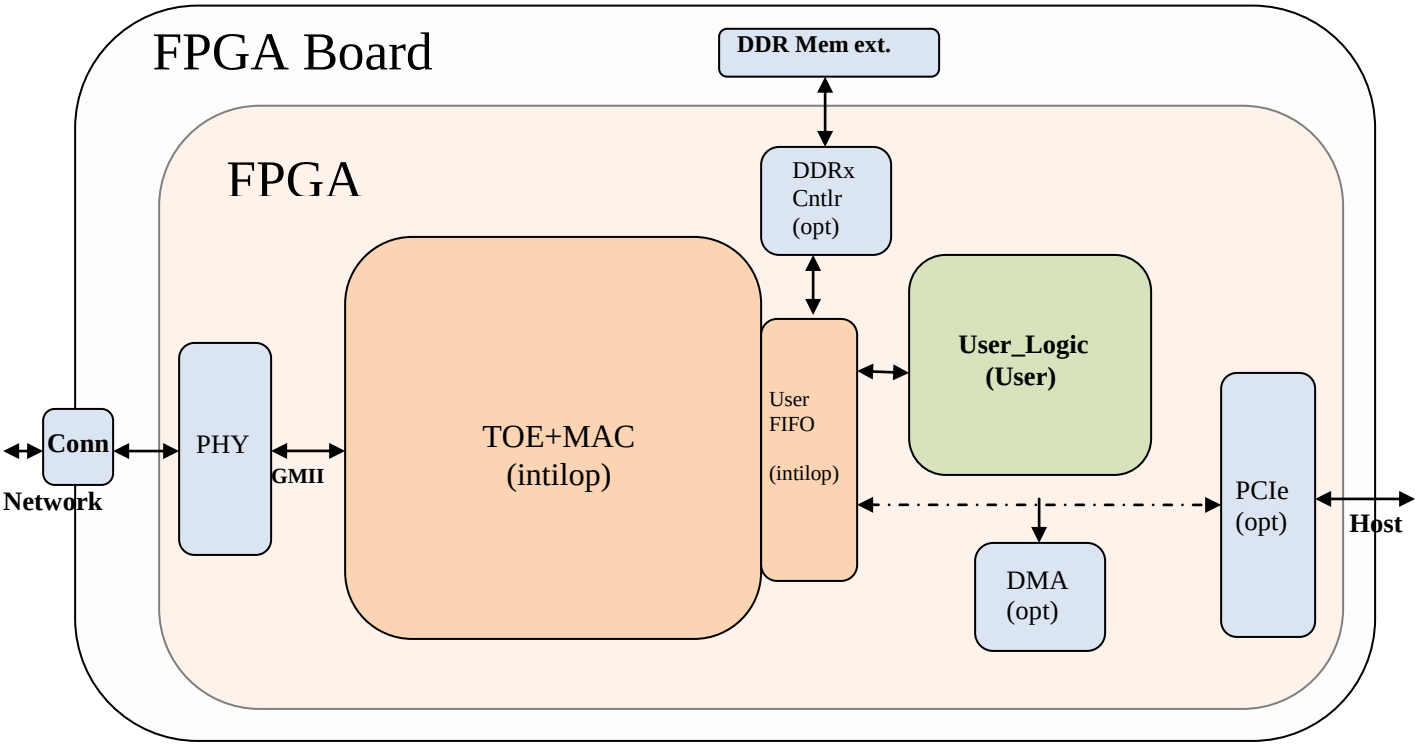
PCI Express IP core and TOE+PCIe FPGA NIC Key features:

- Compliant with the PCI Express® Base Specification, revision 2.0 and 1.1
- Supports Native and Legacy Endpoint: x1, x4, x8 lanes
  - 1 Virtual Channel (VC) with standard TOE+DMA+PCIe NIC System
  - Up to 32 PCIe Virtual Channels available as Option
- Direct TOE Register access via PCIe interface.
- Dedicated and independent high performance TCP Payload Data Path between TOE and PCIe
- TOE-PCIe driver API for easy Linux Host System Application integration
- Standard TOE+PCIe+DMA FPGA-NIC implements up to 4 DMAs.
- Includes Physical, Data Link, Transaction, and EZDMA Application layers
  - Optimized for high throughput and minimal latency
- PIPE interface to PHY
  - 16-bit/125Mhz or 8-bit/250Mhz
- Maximum payload size up to 2KB
- Number of outstanding read requests: up to 16
- Up to 6 BARs plus expansion ROM
- DMA-based user's interface
  - Up to 8 DMA channel option
  - Scatter-Gather support with host based descriptors
  - Integrated DMA arbitration optimized for maximum throughput
  - PCIe Standard Linux Driver with fully Integrated FPGA-NIC-System/development Kit
- Ultra-High Performance, Ultra-low latency PCIe/DMA driver with fully Integrated FPGA-NIC-System/development Kit, available as Option



TOE + DMA + PCIe (Simplified Diagram)



Global System Architecture of TOE in a Xilinx or Altera FPGA

FPGA Development System with fully integrated and tested; PHY+MAC+TOE+PCIe/DMA/Driver available as an option

Specifications brief:

- **Third Gen-TOE. TCP Protocol Compliance and Functionality Proven in multiple networking equipment**
- **Complete header, flag processing of TCP/IP sessions and TCP Payloads in hardware → accelerates by 8x – 15x**
- **TCP Offload Engine- 1-G b/s Wire-speed performance**
- **Scalable to 10 and 40 G b/s**
- **TCP + IP check sum- hardware**
- **TCP segmentation/reassembly in hardware**
- **Multiple 'slot storage' for fragmented packets (opt)**
- **Out of sequence packet detection/storage/Reassembly(opt)**
- **TCP port address tracking/automatic DMA**
- **MAC Address search logic/filter (opt)**
- **IP address search logic/filter (opt)**

- **Accelerate security processing, Storage Networking- TCP**
- **iRDMA implementation- Direct Data placement in Applications buffer --> reduces CPU utilization by 95+ %**
- **Future Proof- Flexible implementation of TCP Offload**
- **Accommodates future Specifications changes.**

AMBA/PLB/AXI CPU interface features;

• Basic transfers
• Various Transfer types
• Master/slave Bus Arbitration (optional)
• Bus slave transactions
• Bus master transactions (optional)
• Address decoder
• Bus Arbiter (optional)
• System Endianness: Little-Endian

Deliverables:

- NetList.
- Test Bench, ,vcd files, configuration code/API for easy Linux port
- Linux PCIe/DMA driver
- Verilog models for various components e.g. TCP/IP Client and Server models, transaction model (optional)
- External memory interface/model (optional).
- TCP Model (optional)
- Verification suite (optional)
- Test packet-traffic suite (optional)

CONTACT INTILOP FOR LATEST SPECIFICATIONS
(Specifications are subject to change)

Technology and Solutions License Purchasing Options:

- **IP Core in Netlist form.**
- **Fully ported and Network tested FPGA development System Platform**
- **IP Customization and Customer Hardware and Application Software integration services.**

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