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10G EMAC (XMAC)
Ultra-Low-Latency

Top Level
Product Specifications

Version 1.0

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General description:

Ultra-High Performance, Ultra-Low-Latency, customizable hardware IP Core. Easily portable to Altera, Xilinx, other FPGAs, Structured ASIC flow and Custom ASICs/SoCs.

INT-10000 is highly flexible that is customizable for layer-2 through Layer-7 network security and network infrastructure and other Data Networking applications. It is recommended for use in, among others, high performance Network security appliances and Network infrastructure appliances. It provides the key IP building block that is designed for easy integration with customer IPs or other standard blocks for mid performance and high performance 10 Giga bit ASICs/SOCs/ASSPs/FPGA-SoCs.

INT-10000 provides capability for enterprises to differentiate their Network security and Network infrastructure appliances from others by implementing differentiated features and Performance parameters.

INT-10000 can process 14M packets for in-line in both directions, simultaneously, at full 10-G-bit rate. The optional Direct write to Memory interface relieves the host CPU from costly DMA/buffer management execution and maintenance tasks.

Rx Latency from Start of Frame till MAC Address Valid → 19.2 ns

Tx Latency from first byte of MAC Address till 'Start of Frame' → 38.4 ns

Full Duplex 100% line rate performance on Rx and Tx sides for 64 byte packets and full size packets…

Features

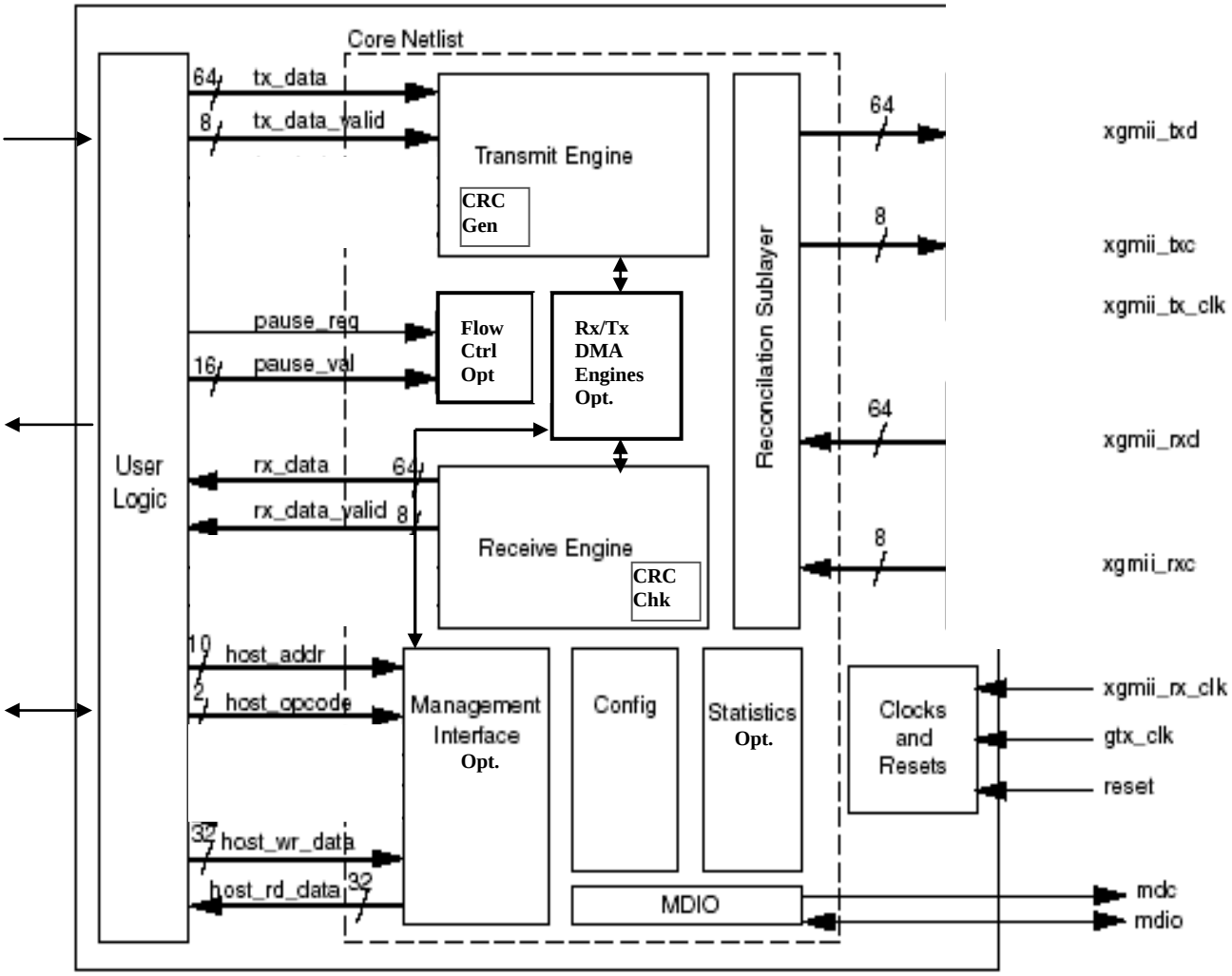
- Ideal for high performance specialized, differentiable ASICs or FPGAs for Network security or Network infrastructure applications for sustained 10G, full-duplex (20G) at 100% utilization rate processing.
- Less than 50,0000 ASIC gates + on-chip memory or 2500 Slices/ALEs
- Designed to interface to either an off-chip PHY device or XAUI LogiCORE (Xilinx) or Altera using the XGMII Interface.
- Separate 64 bit @ 156.25 MHz Read and write host interfaces
- Fully integrated internal RAM block, synthesizable/selectable to 4KB - 256KB. Customizable

- 4/8 intelligent DMA engines. (Opt)
- Direct Memory write and read control block, improves packet receive/transmit performance by 500-1000%, by eliminating software driver to have to manage each frame and manage buffer pointers. (opt)
- Optional, On-chip DDRx or SSRAM memory controller which can address 4K Bytes to 4 MB Bytes on chip or 256 MB off chip memories for packet data storage. (opt)
- Many trade-offs for some functions performed in hardware or software
- Configurable Packet Buffer size from 0KB to 64 KB for RX and Tx.
- Cut-through operation with minimum buffering for maximum flexibility in 64-bit client bus interfacing
- Configurable flow control through MAC Control pause frames that are symmetrically or asymmetrically enabled. Opt.
- Minimum Inter Frame Gap (IFG). standard
- Programmable inter frame gap opt.
- User side interface: AMBA, Simple, MIPs or PPC602xx. Opt.
- Automatic overflow into External Fast SSRAM. (optional)
- Jumbo frame support(opt)
- Same architecture scalable to 40G bps.
- Targeted for Xilinx/Altera, ASIC, Structured ASIC, SoC Integration
- Parameterized design for ASIC or FPGA implementation
- Complete Verification Suite
- High end Switches, Routers, security appliances
- Full 20 G bit Line rate, Packet transfer/Reception- Sustained.
- 14 M, 64 Byte Packets tested through each port
- XGMII interface to PCS
- User configurable Deep FiFOs- 4KB 16k, 32k, 64k, 256k Bytes
- Direct memory storage – interface
- Statistics counters (optional)
- Fully integrated content inspection engine (optional)
- Fully integrated CAM controller/format engine(optional)
- Configurable internal RAM block from 4KB-256KB

Deliverables:

- Netlist; Altera or Xilinx. Source (opt)
- Verilog Models
- Simulation test bench
- Customizable

Internal Block Diagram



10-G Bit Ethernet MAC, with Optional blocks

Core Specifics				
Device Family	**Xilinx- V5, V6** **Altera Str IV, V**			
Speed Grades	**Xilinx- -2, -3** **Altera -2, -3**			
Resources Used[2]	**Slices**	**LUTs**	**FFs**	**Block RAM**
	2267	3560	3655	**0 - 64**
Provided with Core				
Documentation	Product Specification User Guide Getting Started Guide			
Design File Formats	EDIF and NGC netlist			
Constraints File	UCF			
Verification	VHDL test bench Verilog test fixture			
Example Design	VHDL and Verilog			
Design Tool Requirements				
Xilinx- **Altera-**	**Xilinx- ISE 11, 12, 13** **Altera- Quartis 10, 11**			
Simulation	Mentor ModelSim® v6.3c Cadence® IUS v6.1 Synopsys® vcs_mxY-2006.06-SP1			
Synthesis	**Xilinx- ISE 11, 12, 13, Quarts 10, 11**			

Synthesis Estimates:

Manufacturer	Device Number	Frequency (MHz)	Area
Xilinx	xc5vlx110t-2ff1136	156.25	2300 Slices
Xilinx	xc6vlx240t-1ff784	156.25	2300 Slices
Xilinx	xc6vlx240t-3ff784	156.25	2300 Slices
Altera	GX4, GX5	156.25	2100 ALEs

Packet Headers Layer-2 (MAC)

Ethernet Packet Header: (Layer-2)

Preamble	SDF	DA	SA	Length/Type	Payload	CRC

- Preamble: value = 0x55 repeated 7 times (7 bytes)

SDF: Start of Frame Delimiter value = 0xFD (1 byte)

SA: Source MAC Address (6 bytes)

DA: Destination MAC Address (6 bytes)

Length/Type: (2 bytes)

Payload: (64-1500 bytes)

CRC: Cyclic Redundancy Check (4 bytes)